

1.0A SURFACE MOUNT SUPER-FAST RECTIFIER

Features

- Glass Passivated Die Construction
- Super-Fast Recovery Time For High Efficiency
- Low Forward Voltage Drop and High Current Capability
- Surge Overload Rating to 30A Peak
- Ideally Suited for Automated Assembly
- Plastic Material: UL Flammability Classification Rating 94V-0

Mechanical Data

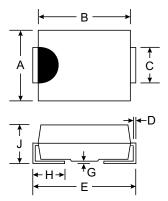
Case: Molded Plastic

 Terminals: Solder Plated Terminal - Solderable per MIL-STD-202, Method 208

• Polarity: Cathode Band or Cathode Notch

Marking: Type Number

Weight: 0.064 grams (approx.)



SMA						
Dim	Min	Max				
Α	2.29	2.92				
В	4.00	4.60				
С	1.27	1.63				
D	0.15	0.31				
E	4.80	5.59				
G	0.10	0.20				
Н	0.76	1.52				
J	2.01	2.62				
All Dimensions in mm						

Maximum Ratings and Electrical Characteristics @ TA = 25°C unless otherwise specified

Single phase, half wave, 60Hz, resistive or inductive load. For capacitive load, derate current by 20%.

Characteristic		Symbol	ES1A	ES1B	ES1C	ES1D	ES1G	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage		V _{RRM} V _{RWM} V _R	50	100	150	200	400	V
RMS Reverse Voltage		V _{R(RMS)}	35	70	105	140	280	٧
Average Rectified Output Current @ T _T = 110°C		lo	1.0					Α
Non-Repetitive Peak Forward Surge Current 8.3ms Single half sine-wave Superimposed on Rated Load (JEDEC Method)		I _{FSM}	30					А
Forward Voltage Drop	@ I _F = 0.6A @ I _F = 1.0A	V _{FM}	0.90 <u> </u>				1.25	V
Peak Reverse Current at Rated DC Blocking Voltage	@ T _A = 25°C @ T _A = 100°C	I _{RM}	5.0 200					μА
Reverse Recovery Time (Note 3)		t _{rr}			20			ns
Typical Junction Capacitance (Note 2)		Cj			10			pF
Typical Thermal Resistance, Junction to Terminal (Note 1)		$R_{\theta JT}$	40					K/W
Operating and Storage Temperature Range		T _{j,} T _{STG}	-65 to +150					°C

Notes

- 1. Unit mounted on PC board with 5.0 mm² (0.013 mm thick) copper pad as heat sink.
- 2. Measured at 1.0MHz and applied reverse voltage of 4.0V DC.
- 3. Measured with $I_F = 0.5A$, $I_R = 1.0A$, $I_{rr} = 0.25A$. See figure 5.

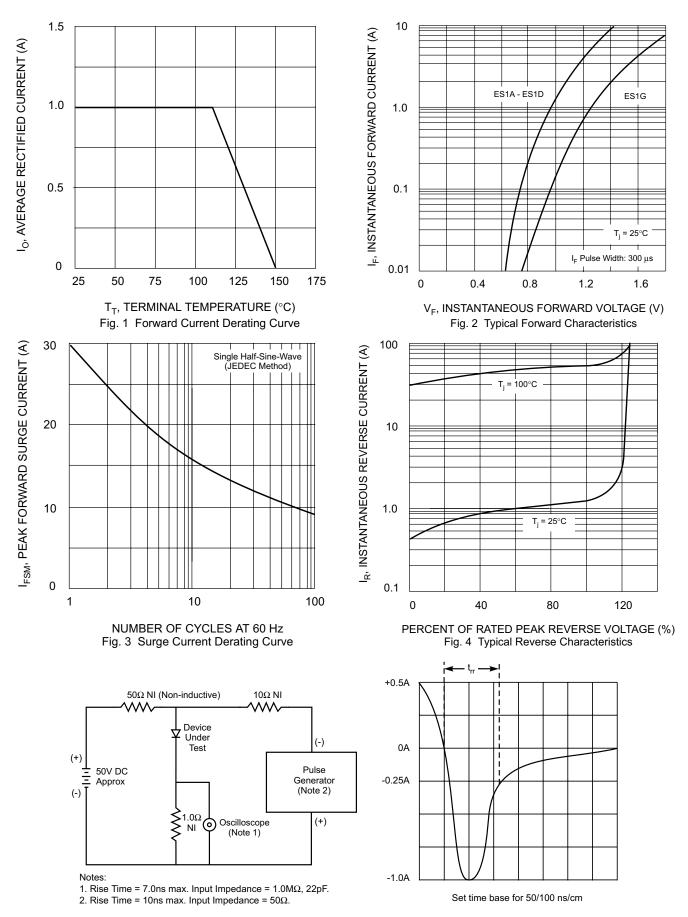


Fig. 5 Reverse Recovery Time Characteristic and Test Circuit