256-Position Two-Time Programmable I²C Digital Potentiometer

Preliminary Technical Data

AD5170

FEATURES

256-position
TTP(Two-Time Programmable) Set-and-Forget sesistance setting allows second chance permanent programming
End-to-end resistance 2.5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ
Compact MSOP-10 (3 mm × 4.9 mm) Package
Fast Settling Time: t_S = 5µs Typ in Power-Up
Full read/write of wiper register
Power-on preset to midscale
Extra package address decode pins AD0 and AD1
Computer Software Replaces µC in Factory Programming Applications
Single supply 2.7 V to 5.5 V
Low temperature coefficient 35 ppm/°C
Low power, I_{DD} = 5 µA
Wide operating temperature –40°C to +125°C
Evaluation board available

APPLICATIONS

Systems Calibrations
Electronics Level Settings
Mechanical Trimmers® Replacement in New Designs
Permamenent Factory PCB Setting
Transducer adjustment of pressure, temperature, position, chemical, and optical sensors
RF amplifier biasing
Automotive electronics adjustment
Gain control and offset adjustment

GENERAL OVERVIEW

The AD5170 is a 256-position, Two-Time Programmable(TTP) digital potentiometer that employs fuse link technology to enable *two* opportunities at permanently programming the resistance setting. This device performs the same electronic adjustment function as mechanical potentiometers or variable resistors, with enhanced resolution, solid-state reliability, and superior low temperature coefficient performance.

The AD5170 is controlled using a 2-wire, I²C compatible digital interface. It allows unlimited adjustments before "permanently"(you really have two opportunities) setting the resistance value. After the final value is determined, a fuse blow command is executed which freezes the wiper position(analogous to placing epoxy on a mechanical trimmer).

In addition, for applications that program the AD5170 at the factory, Analog Devices offers device programming software running on Windows® NT, 2000, and XP operating systems. This software effectively replaces any external I²C controllers, which in turn enhances users' systems time-to-market.

An AD5170 evaluation kit and software are available. The kit includes the connector and cable that can be converted for further factory programming applications.

FUNCTIONAL BLOCK DIAGRAMS

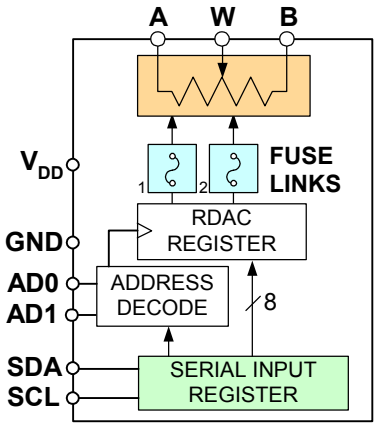

Figure 1. AD5170

Note:
The terms *digital potentiometer*, *VR*, and *RDAC* are used interchangeably.

Rev. PrE7/9/03

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TABLE OF CONTENTS

REVISION HISTORY

Revision 0: Initial Version

ELECTRICAL CHARACTERISTICS—2.5 kΩ VERSION

(V_{DD} = 5 V ± 10%, or 3 V ± 10%; V_A = +V_{DD}; V_B = 0 V; –40°C < T_A < +125°C; unless otherwise noted.)

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect	–1.5	±0.1	+1.5	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	–4	±0.75	+4	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = 25°C	–30		+30	%
Resistance Temperature Coefficient	$\Delta R_{AB}/\Delta T$	V_{AB} = V_{DD}, Wiper = no connect		35		ppm/°C
Wiper Resistance	R_W			50	120	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (Specifications apply to all VRs)						
Resolution	N				8	Bits
Differential Nonlinearity[4]	DNL		–1.5	±0.1	+1.5	LSB
Integral Nonlinearity[4]	INL		–1.5	±0.6	+1.5	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 0x80		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0xFF	–6	–2.5	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	+2	+6	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A,B,W}$		GND		V_{DD}	V
Capacitance[6] A, B	$C_{A,B}$	f = 1 MHz, measured to GND, Code = 0x80		45		pF
Capacitance[6] W	C_W	f = 1 MHz, measured to GND, Code = 0x80		60		pF
Shutdown Supply Current[7]	I_{DD_SD}	V_{DD} = 5.5 V		0.01	1	µA
Common-Mode Leakage	I_{CM}	V_A = V_B = V_{DD}/2		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}		2.4			V
Input Logic Low	V_{IL}				0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		3	5	µA
Power Dissipation[8]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			0.2	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = +5 V ± 10%, Code = Midscale		±0.02	±0.05	%/%
DYNAMIC CHARACTERISTICS[6, 9]						
Bandwidth –3dB	BW_5K	R_{AB} = 2.5 kΩ, Code = 0x80		2.4		MHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz		0.05		%
V_W Settling Time	t_S	V_A= 5 V, V_B = 0 V, ±1 LSB error band		1		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 2.5 kΩ, RS = 0		4.5		nV/√Hz

ELECTRICAL CHARACTERISTICS—10 kΩ, 50 kΩ, 100 kΩ VERSIONS

(V_{DD} = 5 V ± 10%, or 3 V ± 10%; $V_A = V_{DD}$; V_B = 0 V; –40°C < T_A < +125°C; unless otherwise noted.)

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect	–1	±0.1	+1	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	–2	±0.25	+2	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = 25°C	–30		+30	%
Resistance Temperature Coefficient	$\Delta R_{AB}/\Delta T$	$V_{AB} = V_{DD}$, Wiper = no connect		35		ppm/°C
Wiper Resistance	R_W	V_{DD} = 5 V		50	120	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (Specifications apply to all VRs)						
Resolution	N				8	Bits
Differential Nonlinearity[4]	DNL		–1	±0.1	+1	LSB
Integral Nonlinearity[4]	INL		–1	±0.3	+1	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 0x80		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0xFF	–3	–1	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	1	3	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A,B,W}$		GND		V_{DD}	V
Capacitance[6] A, B	$C_{A,B}$	f = 1 MHz, measured to GND, Code = 0x80		45		pF
Capacitance[6] W	C_W	f = 1 MHz, measured to GND, Code = 0x80		60		pF
Shutdown Supply Current[7]	I_{DD_SD}	V_{DD} = 5.5 V		0.01	1	µA
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_{DD}/2$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}		2.4			V
Input Logic Low	V_{IL}				0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		3	5	µA
Power Dissipation[8]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			0.2	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = +5 V ± 10%, Code = Midscale		±0.02	±0.05	%/%
DYNAMIC CHARACTERISTICS[6, 9]						
Bandwidth –3dB	BW	R_{AB} = 10 kΩ/50 kΩ/100 kΩ, Code = 0x80		600/100/40		kHz
Total Harmonic Distortion	THD_W	V_A =1 V rms, V_B = 0 V, f = 1 kHz, R_{AB} = 10 kΩ		0.05		%
V_W Settling Time (10 kΩ/50 kΩ/100 kΩ)	t_S	V_A = 5 V, V_B = 0 V, ±1 LSB error band		2		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 5 kΩ, RS = 0		9		nV/√Hz

TIMING CHARACTERISTICS—2.5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ VERSIONS

(V_{DD} = +5V ± 10%, or +3V ± 10%; $V_A = V_{DD}$; V_B = 0 V; –40°C < T_A < +125°C; unless otherwise noted.)

Table 3.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
I²C INTERFACE TIMING CHARACTERISTICS[6, 10] (Specifications Apply to All Parts)						
SCL Clock Frequency	f_{SCL}				400	kHz
t_{BUF} Bus Free Time between STOP and START	t_1		1.3			µs
$t_{HD;STA}$ Hold Time (Repeated START)	t_2	After this period, the first clock pulse is generated.	0.6			µs
t_{LOW} Low Period of SCL Clock	t_3		1.3			µs
t_{HIGH} High Period of SCL Clock	t_4		0.6		50	µs
$t_{SU;STA}$ Setup Time for Repeated START Condition	t_5		0.6			µs
$t_{HD;DAT}$ Data Hold Time	t_6				0.9	µs
$t_{SU;DAT}$ Data Setup Time	t_7		100			ns
t_F Fall Time of Both SDA and SCL Signals	t_8				300	ns
t_R Rise Time of Both SDA and SCL Signals	t_9				300	ns
$t_{SU;STO}$ Setup Time for STOP Condition	t_{10}		0.6			µs

NOTES
[1] Typical specifications represent average readings at +25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
[3] $V_{AB} = V_{DD}$, Wiper (V_W) = no connect.
[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. VA = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor terminals A, B, W have no limitations on polarity with respect to each other.
[6] Guaranteed by design and not subject to production test.
[7] Measured at the A terminal. The A terminal is open circuited in shutdown mode.
[8] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.
[9] All dynamic characteristics use V_{DD} = 5 V.
[10] See timing diagrams for locations of measured values.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C, unless otherwise noted.)

Table 4.

Parameter	Value
V_{DD} to GND	–0.3 V to +7 V
V_A, V_B, V_W to GND	V_{DD}
I_{MAX}[1]	±20 mA
Digital Inputs and Output Voltage to GND	0 V to +7 V
Operating Temperature Range	–40°C to +125°C
Maximum Junction Temperature (T_{JMAX})	150°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Thermal Resistance[2] θ_{JA}: MSOP-10	230°C/W

NOTES
[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.
[2] Package power dissipation = ($T_{JMAX} - T_A$)/θ_{JA}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS

TEST CIRCUITS

Figure 2 to Figure 10 illustrate the test circuits that define the test conditions used in the product specification tables.

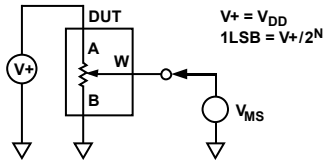

Figure 2. Test Circuit for Potentiometer Divider Nonlinearity Error (INL, DNL)

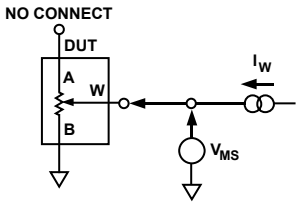

Figure 3. Test Circuit for Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

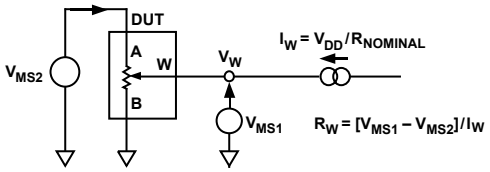

Figure 4. Test Circuit for Wiper Resistance

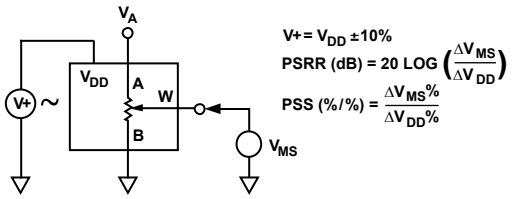

Figure 5. Test Circuit for Power Supply Sensitivity (PSS, PSSR)

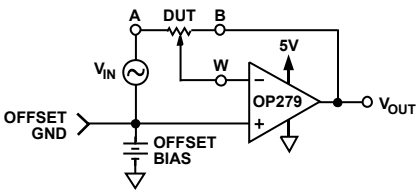

Figure 6. Test Circuit for Inverting Gain

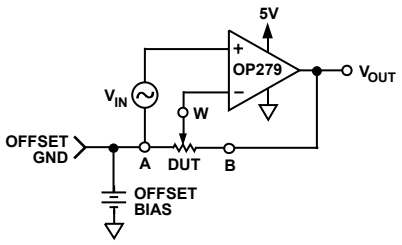

Figure 7. Test Circuit for Noninverting Gain

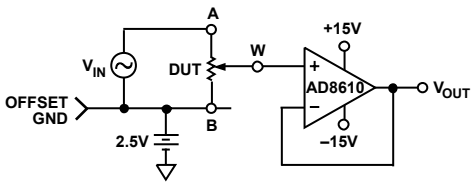

Figure 8. Test Circuit for Gain vs. Frequency

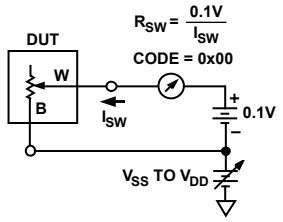

Figure 9. Test Circuit for Incremental ON Resistance

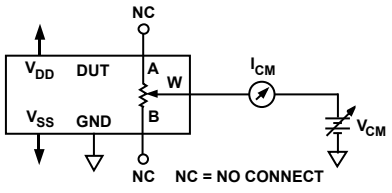

Figure 10. Test Circuit for Common-Mode Leakage current

I²C INTERFACE

Table 5. Write Mode

S	0	1	0	1	1	AD1	AD0	$\overline{W}$	A	2T	SD	T	0	OV	X	X	X	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Instruction Byte									Data Byte									

Table 6. Read Mode

S	0	1	0	1	1	AD1	AD0	R	A	D7	D6	D5	D4	D3	D2	D1	D0	A	E1	E0	X	X	X	X	X	X	A	P
	Slave Address Byte									Instruction Byte									Data Byte									

S = Start Condition

P = Stop Condition

A = Acknowledge

X = Don't Care

$\overline{W}$ = Write

R = Read

2T = Second fuse link array for Two Time Programming. Logic 0 corresponds to first trim. Logic 1 corresponds to second trim.

SD = Shutdown connects wiper to B terminal and open circuits A terminal. It does not change contents of wiper register.

T = OTP Programming Bit. Logic 1 programs wiper permanently.

OV = Overwrite fuse setting and program digital pot to different setting. Note that upon power up, digital pot will preset to either midscale or fuse setting depending on whether or not the fuse link has been blown.

D7, D6, D5, D4, D3, D2, D1, D0 = Data Bits

E1, E0 = OTP Validation Bits

0 , 0 = Ready to program

0 , 1 = Test fuse not blown successfully(check setup)

1 , 0 = Fatal error. Retry.

1 , 1 =Programmed Successfully. No further adjustments possible.

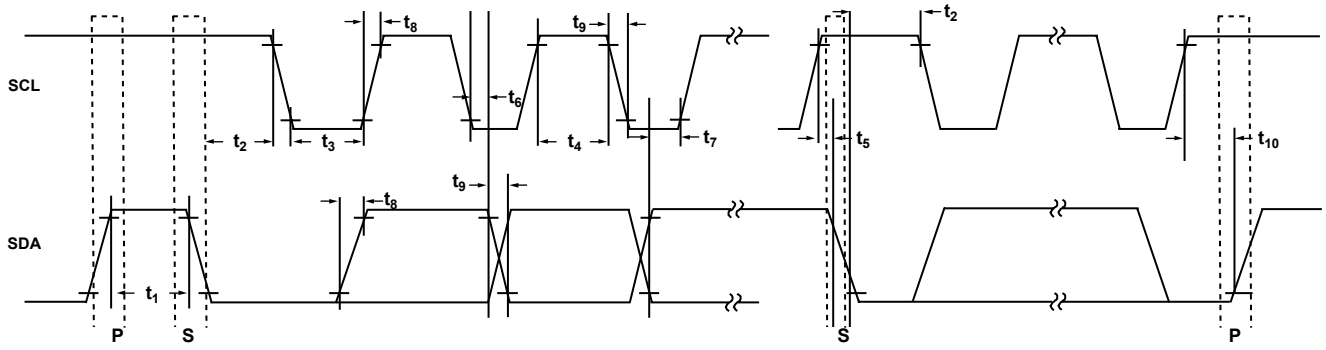

Figure 11. I²C Interface Detailed Timing Diagram

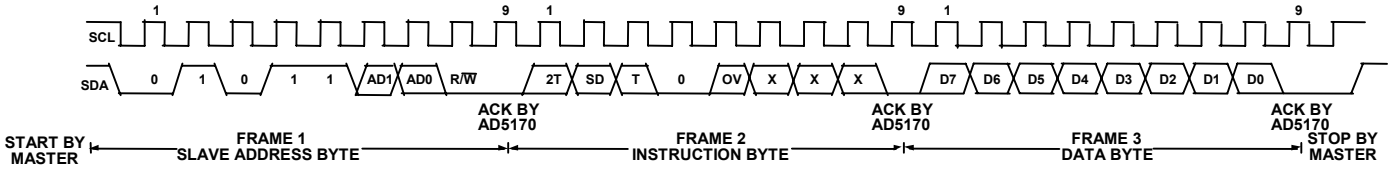

Figure 12. Writing to the RDAC Register

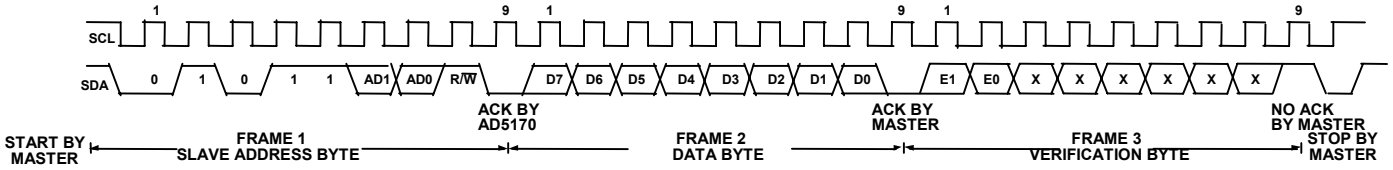

Figure 13 Reading Data from the RDAC Register

OPERATION

The AD5170 is a 256-position digitally controlled variable resistor (VR) device.

An internal power-on preset places the wiper at midscale during power-on, which simplifies the fault condition recovery at power-up.

If the device has been permanently programmed via the fuse link technology, the device will power up at that permanent setting.

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistance of the RDAC between terminals A and B is available in 5 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ. The final two or three digits of the part number determine the nominal resistance value, e.g., 10 kΩ = 10; 50 kΩ = 50. The nominal resistance (R_{AB}) of the VR has 256 contact points accessed by the wiper terminal, plus the B terminal contact. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible settings. Assume a 10 kΩ part is used, the wiper's first connection starts at the B terminal for data 0x00. Since there is a 60 Ω wiper contact resistance, such connection yields a minimum of 60 Ω resistance between terminals W and B. The second connection is the first tap point, which corresponds to 99 Ω (R_{WB} = R_{AB}/256 + R_W = 39 Ω + 60 Ω) for data 0x01. The third connection is the next tap point, representing 138 Ω (2 × 39 Ω + 60 Ω) for data 0x02, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 9961 Ω (R_{AB} – 1 LSB + R_W). Figure 14 shows a simplified diagram of the equivalent RDAC circuit where the last resistor string will not be accessed; therefore, there is 1 LSB less of the nominal resistance at full scale in addition to the wiper resistance.

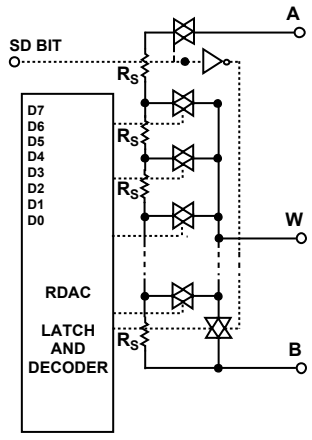

Figure 14. AD5170 Equivalent RDAC Circuit

The general equation determining the digitally programmed output resistance between W and B is

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + R_W \quad (1)$$

where D is the decimal equivalent of the binary code loaded in the 8-bit RDAC register, R_{AB} is the end-to-end resistance, and R_W is the wiper resistance contributed by the on resistance of the internal switch.

In summary, if R_{AB} = 10 kΩ and the A terminal is open circuited, the following output resistance R_{WB} will be set for the indicated RDAC latch codes.

Table 7. Codes and Corresponding R_{WB} Resistance

D (Dec.)	R_{WB} (Ω)	Output State
255	9,961	Full Scale (R_{AB} – 1 LSB + R_W)
128	5,060	Midscale
1	99	1 LSB
0	60	Zero Scale (Wiper Contact Resistance)

Note that in the zero-scale condition a finite wiper resistance of 60 Ω is present. Care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the wiper W and terminal A also produces a digitally controlled complementary resistance R_{WA}. When these terminals are used, the B terminal can be opened. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{256} \times R_{AB} + R_W \quad (2)$$

For R_{AB} = 10 kΩ and the B terminal open circuited, the following output resistance R_{WA} will be set for the indicated RDAC latch codes.

Table 8. Codes and Corresponding R_{WA} Resistance

D (Dec.)	R_{WA} (Ω)	Output State
255	99	Full Scale
128	5,060	Midscale
1	9,961	1 LSB
0	10,060	Zero Scale

Typical device to device matching is process lot dependent and may vary by up to ±30%. Since the resistance element is

processed in thin film technology, the change in R_{AB} with temperature has a very low 45 ppm/°C temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper-to-B and wiper-to-A proportional to the input voltage at A-to-B. Unlike the polarity of V_{DD} to GND, which must be positive, voltage across A-B, W-A, and W-B can be at either polarity.

If ignoring the effect of the wiper resistance for approximation, connecting the A terminal to 5 V and the B terminal to ground produces an output voltage at the wiper-to-B starting at 0 V up to 1 LSB less than 5 V. Each LSB of voltage is equal to the voltage applied across terminal AB divided by the 256 positions of the potentiometer divider. The general equation defining the output voltage at V_W with respect to ground for any valid input voltage applied to terminals A and B is

$$V_W(D) = \frac{D}{256}V_A + \frac{256-D}{256}V_B \quad (3)$$

For a more accurate calculation, which includes the effect of wiper resistance, V_W, can be found as

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}}V_A + \frac{R_{WA}(D)}{R_{AB}}V_B \quad (4)$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors R_{WA} and R_{WB} and not the absolute values. Therefore, the temperature drift reduces to 15 ppm/°C.

I²C COMPATIBLE 2-WIRE SERIAL BUS

The 2-wire I²C serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, which is when a high-to-low transition on the SDA line occurs while SCL is high. The following byte is the slave address byte, which consists of the slave address followed by an R/$\overline{W}$ bit (this bit determines whether data will be read from or written to the slave device). AD0 and AD1 are configurable address bits which allow up to four devices on one bus(see Table 5).

   The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register. If the R/$\overline{W}$ bit is high, the master will read from the slave device. On the other hand, if the R/$\overline{W}$ bit is low, the master will write to the slave device.

2. In the write mode, the second byte is the instruction byte. The first bit (MSB), 2T, of the instruction byte is the second trim enable bit. A logic low will select trim#1 and a logic high will select trim#2. This means that after blowing the fuses with trim#1, you still have another chance to blow them again w/ trim #2. Note that using trim#2 before trim#1 will effectively disable trim#1 and in turn only allow one time programming.

   The second MSB, SD, is a shutdown bit. A logic high causes an open circuit at terminal A while shorting the wiper to terminal B. This operation yields almost 0 Ω in rheostat mode or 0 V in potentiometer mode. It is important to note that the shutdown operation does not disturb the contents of the register. When brought out of shutdown, the previous setting will be applied to the RDAC. Also, during shutdown, new settings can be programmed. When the part is returned from shutdown, the corresponding VR setting will be applied to the RDAC.

   The third MSB, T, is the OTP(One Time Programmable) programming bit. A logic high blows the poly fuses and programs the resistor setting permanently. For example, if you wanted to use blow the first array of fuses, the instruction byte would be 00100XXX. If you wanted to blow the second array of fuses, your instruction byte would be 10100XXX. A logic low of the T bit simply allows the device to act as a typical volatile digital potentiometer.

   The fourth MSB must always be at a logic zero.

   The fifth MSB, OW, is an overwrite bit. When raised to a logic high, this bit allows the RDAC setting to be changed even after the internal fuses have been blown. However, once the OW bit is returned to a logic zero, the position of the RDAC will return to the setting prior to overwrite. Because OW is not static, if the device is powered off and on, the RDAC will preset to midscale or to the setting at which the fuses were blown depending on whether or not the fuses have been permanently set already.

   The remainder of the bits in the instruction byte are don't cares(see Table 5).

   After acknowledging the instruction byte, the last byte in write mode is the data byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Table 5).

3. In the read mode, the data byte follows immediately after

the acknowledgment of the slave address byte. Data is transmitted over the serial bus in sequences of nine clock pulses(a slight difference with the write mode, where there are eight data bits followed by an acknowledge bit). Similarly, the transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 13).

Following the data byte, the validation byte contains two validation bits, E0 and E1. These bits signify the status of the One Time Programming(see Table 9).

4. After all data bits have been read or written, a STOP condition is established by the master. A STOP condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master will pull the SDA line high during the tenth clock pulse to establish a STOP condition. In read mode, the master will issue a No Acknowledge for the ninth clock pulse (i.e., the SDA line remains high). The master will then bring the SDA line low before the tenth clock pulse which goes high to establish a STOP condition (see Figure 13).

A repeated write function gives the user flexibility to update the RDAC output a number of times after addressing and instructing the part only once. For example, after the RDAC has acknowledged its slave address and instruction bytes in the write mode, the RDAC output will update on each successive byte. If different instructions are needed, the write/read mode has to start again with a new slave address, instruction, and data byte. Similarly, a repeated read function of the RDAC is also allowed.

Table 9. Validation Status

E1	E0	Status
0	0	Ready for Programming
0	1	Test Fuse Not Blown Successfully (Check Setup)
1	0	Fatal Error. Some Fuses are not Blown. Retry Again
1	1	Successful. No Further Programming is Possible

Multiple Devices on One Bus

Figure 15 shows four AD5170 devices on the same serial bus. Each has a different slave address since the states of their AD0 and AD1 pins are different. This allows each device on the bus to be written to or read from independently. The master device output bus line drivers are open-drain pull-downs in a fully I²C compatible interface.

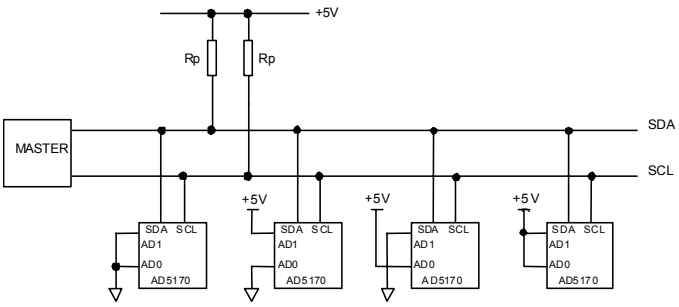

Figure 15. Multiple AD5170 Devices on One I²C Bus

LEVEL SHIFTING FOR BIDIRECTIONAL INTERFACE

While most legacy systems may be operated at one voltage, a new component may be optimized at another. When two systems operate the same signal at two different voltages, proper level shifting is needed. For instance, one can use a 3.3 V E²PROM to interface with a 5 V digital potentiometer. A level shifting scheme is needed to enable a bidirectional communication so that the setting of the digital potentiometer can be stored to and retrieved from the E²PROM. Figure 16 shows one of the implementations. M1 and M2 can be any N-channel signal FETs, or if V_{DD} falls below 2.5 V, low threshold FETs such as the FDV301N.

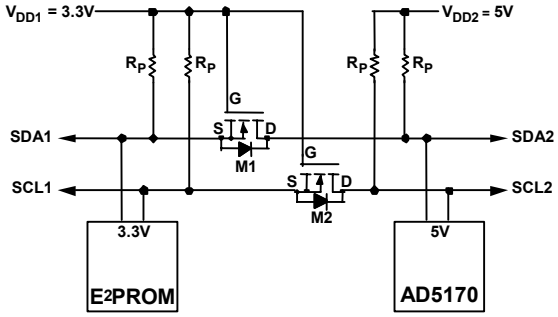

Figure 16. Level Shifting for Operation at Different Potentials

ESD PROTECTION

All digital inputs are protected with a series input resistor and parallel Zener ESD structures shown in Figure 17 and Figure 18. This applies to the digital input pins SDA, SCL, and AD0.

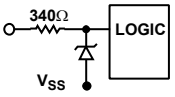

Figure 17. ESD Protection of Digital Pins

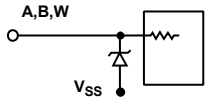

Figure 18. ESD Protection of Resistor Terminals

TERMINAL VOLTAGE OPERATING RANGE

The AD5172/73 V_{DD} and GND power supply defines the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on terminals A, B, and W that exceed V_{DD} or GND will be clamped by the internal forward biased diodes (see Figure 19).

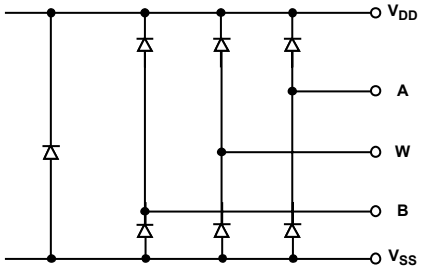

Figure 19. Maximum Terminal Voltages Set by V_{DD} and V_{SS}

POWER-UP SEQUENCE

Since the ESD protection diodes limit the voltage compliance at terminals A, B, and W (see Figure 19), it is important to power V_{DD}/GND before applying any voltage to terminals A, B, and W; otherwise, the diode will be forward biased such that V_{DD} will be powered unintentionally and may affect the rest of the user's circuit. The ideal power-up sequence is in the following order: GND, V_{DD}, digital inputs, and then $V_{A/B/W}$. The relative order of powering V_A, V_B, V_W, and the digital inputs is not important as long as they are powered after V_{DD}/GND.

POWER SUPPLY CONSIDERATIONS

AD5170 employs fuse link technology, which requires an adequate current density to blow the internal fuses to achieve a given setting. As a result, the power supply, either an on-board linear regulator or rack-mount power supply, must be rated at 5V with less than ±5% tolerance. The supply should be able to handle 100mA of transient current, which lasts about 400 ms during the one-time programming. A low ESR 1uF to 10uF tantalum or electrolytic bypass capacitor should be applied to V_{DD} to minimize the transient disturbances during the programming as shown. Once the programming is completed, the supply voltage can be reduced to 2.7V with a supply current as low as 1uA.

For users who have an on-board 3V supply for portable applications, a separate 5V supply must be applied one time in the factories for programming and a low VF Schotky Diode should be designed with the AD5170 to isolate the supply voltages. Once the programming is done, the 5V supply can be removed and V_{DD} reduced to 2.7V for minimum operation.

LAYOUT AND POWER SUPPLY BYPASSING

It is a good practice to employ compact, minimum lead length layout design. The leads to the inputs should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also a good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with disc or chip ceramic capacitors of 0.01 µF to 0.1 µF. Low ESR 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at the supplies to minimize any transient disturbance and low frequency ripple (see Figure 20). Note that the digital ground should also be joined remotely to the analog ground at one point to minimize the ground bounce.

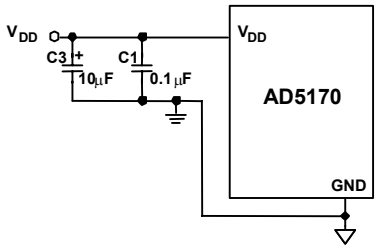

Figure 20. Power Supply Bypassing

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

PIN CONFIGURATION

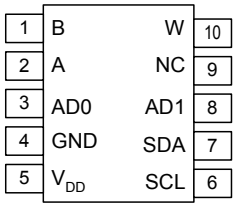

Figure 21.- Pin Configuration

Table 10. Pin Configuration

Pin	Name	Description
1	B	B Terminal.
2	A	A Terminal.
3	AD0	Programmable address bit 0 for multiple package decoding.
4	GND	Digital Ground.
5	V_{DD}	Positive Power Supply..
6	SCL	Serial Clock Input. Positive edge triggered.
7	SDA	Serial Data Input/Output.
8	AD1	Programmable address bit 1 for multiple package decoding.
9	NC	No Connect.
10	W	W Terminal.

OUTLINE DIMENSIONS

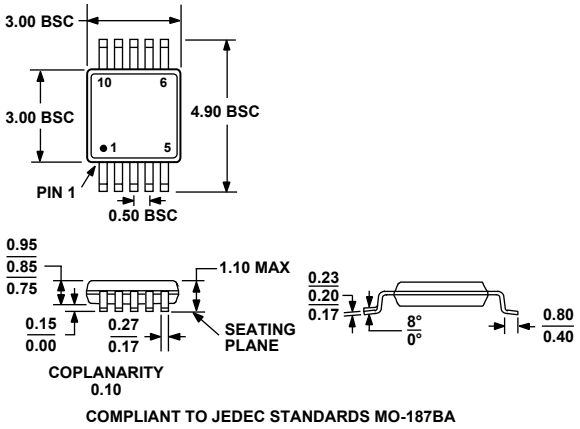

Figure 22. 10-Lead Mini Small Outline Package [MSOP] (RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	R_{AB} (Ω)	Temperature	Package Description	Package Option	Branding
AD5170BRM2.5-R2	2.5k	–40°C to +125°C	MSOP-10	RM-10	D0Y
AD5170BRM2.5-RL7	2.5k	–40°C to +125°C	MSOP-10	RM-10	D0Y
AD5170BRM10-R2	10k	–40°C to +125°C	MSOP-10	RM-10	D0Z
AD5170BRM10-RL7	10k	–40°C to +125°C	MSOP-10	RM-10	D0Z
AD5170BRM50-R2	50k	–40°C to +125°C	MSOP-10	RM-10	D0W
AD5170BRM50-RL7	50k	–40°C to +125°C	MSOP-10	RM-10	D0W
AD5170BRM100-R2	100k	–40°C to +125°C	MSOP-10	RM-10	D0X
AD5170BRM100-RL7	100k	–40°C to +125°C	MSOP-10	RM-10	D0X
AD5170EVAL	See Note 1		Evaluation Board		

[1]The evaluation board is shipped with the 10 kΩ R_{AB} resistor option; however, the board is compatible with all available resistor value options.

The AD5170 contains 2532 transistors. Die size: 30.7 mil × 76.8 mil = 2,358 sq. mil.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.