

MM54HCT107/MM74HCT107

Dual J-K Flip-Flops with Clear

General Description

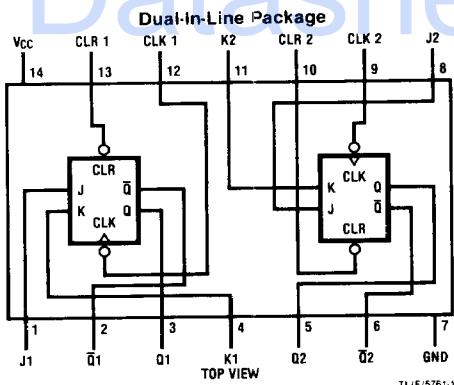
The MM54HCT107/MM74HCT107 utilize silicon gate CMOS technology. They have input threshold and output drive similar to LS-TTL with the low standby power of CMOS.

These flip-flops have independent J, K, clear and clock inputs and Q and \bar{Q} outputs. The flip-flops are edge-triggered and change state on the negative-going transition of the clock pulse. Clear is independent of the clock and accomplished by a low level on the input.

All inputs to this device are protected from damage due to electrostatic discharge by diodes to V_{CC} and ground.

PRELIMINARY


Connection Diagram



MM54HCT/MM74HCT devices are intended to interface TTL and NMOS components to CMOS components. When there is a LS-TTL equivalent, these parts can be used as plug-in replacements to reduce system power consumption in existing designs.

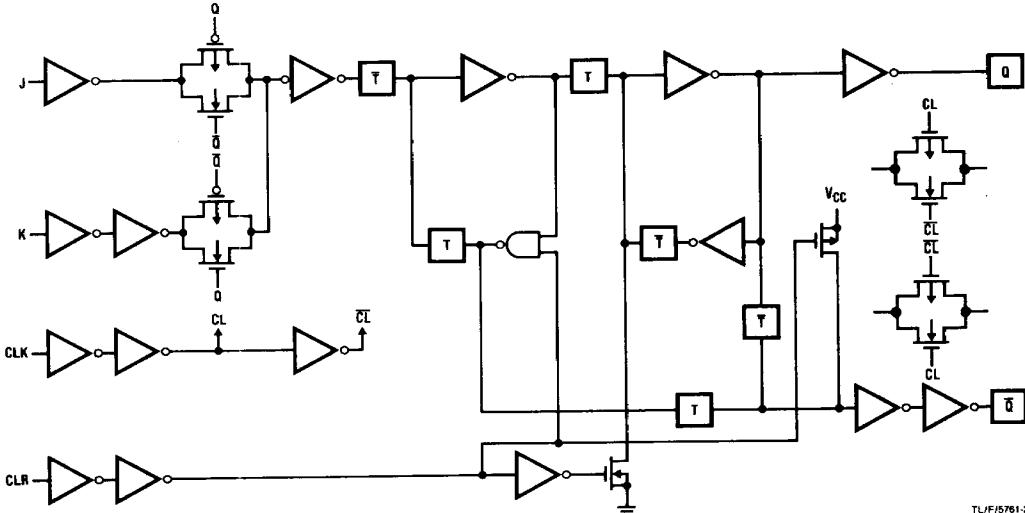
Features

- Typical propagation delay: 20 ns
- Low quiescent current 8 μ A maximum (74HCT Series)
- Fanout of 10 LS-TTL loads

Truth Table

Inputs				Outputs	
CLR	CLK	J	K	Q	\bar{Q}
L	X	X	X	L	H
H	↓	L	L	Q ₀	\bar{Q}_0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q ₀	\bar{Q}_0

Logic Diagram



Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Voltage (V_{IN})	-1.5V to $V_{CC} + 1.5V$
DC Output Voltage (V_{OUT})	-0.5V to $V_{CC} + 0.5V$
Clamp Diode Current (I_{IK}, I_{OK})	$\pm 20\text{ mA}$
DC Output Current, per Pin (I_{OUT})	$\pm 25\text{ mA}$
DC V_{CC} or GND Current, per Pin (I_{CC})	$\pm 50\text{ mA}$
Storage Temperature Range (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HCT	-40	+85	°C
MM54HCT	-55	+125	°C
Input Rise or Fall Times (t_r, t_f)	500	ns	

DC Electrical Characteristics $V_{CC} = 5V \pm 10\%$ unless otherwise specified

Symbol	Parameter	Conditions	$T_A = 25^\circ\text{C}$		74HCT	54HCT	Units
			Typ		$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	$T_A = -55^\circ\text{C to } 125^\circ\text{C}$	
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} = 20\text{ }\mu\text{A}$ $ I_{OUT} = 4.0\text{ mA}, V_{CC} = 4.5V$ $ I_{OUT} = 4.8\text{ mA}, V_{CC} = 5.5V$	V_{CC} 4.2 5.7	$V_{CC} - 0.1$ 3.98 4.98	$V_{CC} - 0.1$ 3.84 4.84	$V_{CC} - 0.1$ 3.7 4.7	V V V
V_{OL}	Maximum Low Level Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} = 20\text{ }\mu\text{A}$ $ I_{OUT} = 4.0\text{ mA}, V_{CC} = 4.5V$ $ I_{OUT} = 4.8\text{ mA}, V_{CC} = 5.5V$	0 0.2 0.2	0.1 0.26 0.26	0.1 0.33 0.33	0.1 0.4 0.4	V V V
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND, V_{IH} or V_{IL}		± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $ I_{OUT} = 0\text{ }\mu\text{A}$		4.0	40	80	μA
		$V_{IN} = 2.4V$ or $0.5V$ (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power dissipation temperature derating—plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin, all other inputs held at V_{CC} or GND.**AC Electrical Characteristics** $V_{CC} = 5V, T_A = 25^\circ\text{C}, C_L = 15\text{ pF}, t_r = t_f = 6\text{ ns}$ (Note 6)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q or \bar{Q}		18	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clear to Q or \bar{Q}		18	30	ns
t_{REM}	Minimum Removal Time, Clear to Clock			20	ns
t_s	Minimum Set-Up Time J or K Clock		10	20	ns
t_H	Minimum Hold Time Clock to J or K		-3	0	ns
t_W	Minimum Pulse Width Clock, Clear		8	16	ns

AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$, $C_L = 50 \text{ pF}$, $t_r = t_f = 6 \text{ ns}$ unless otherwise specified

Symbol	Parameter	Conditions	$T_A = 25^\circ\text{C}$		74HCT $T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	54HCT $T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	Units
			Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency			27	22	18	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q or \bar{Q}		22	35	44	52	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clear to Q or \bar{Q}		22	35	44	52	ns
t_{REM}	Minimum Removal Time Clear to Clock			20	25	30	ns
t_s	Minimum Set-Up Time J or K to Clock		10	20	25	30	ns
t_H	Minimum Hold Time Clock to J or K		-3	0	0	0	ns
t_W	Minimum Pulse Width Clock or Clear			16	20	24	ns
t_r, t_f	Maximum Input Rise and Fall Time			500	500	500	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(Per Flip-Flop)					pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.