

74LVT573

3.3 V octal D-type transparent latch; 3-state

Rev. 8 — 22 November 2011

Product data sheet

1. General description

The 74LVT573 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V. This device is an octal transparent latch coupled to eight 3-state output buffers. The two sections of the device are controlled independently by Latch Enable (LE) and Output Enable (\overline{OE}) control gates. The 74LVT573 has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

The data on the Dn inputs are transferred to the latch outputs when the Latch Enable (LE) input is High. The latch remains transparent to the data inputs while LE is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-state output buffers are designed to drive heavily loaded 3-state buses, MOS memories, or MOS microprocessors. The active-Low Output Enable (\overline{OE}) controls all eight 3-state buffers independent of the latch operation.

When \overline{OE} is Low, the latched or transparent data appears at the outputs. When \overline{OE} is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

2. Features and benefits

- Inputs and outputs arranged for easy interfacing to microprocessors
- 3-state outputs for bus interfacing
- Common output enable control
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- No bus current loading when output is tied to 5 V bus
- Power-up reset
- Power-up 3-state
- Latch-up protection
 - ◆ JESD78 class II exceeds 500 mA
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$



3. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|-------------|-------------------|----------|---|----------|
| | Temperature range | Name | Description | |
| 74LVT573D | -40 °C to +85 °C | SO20 | plastic small outline package; 20 leads; body width 7.5 mm | SOT163-1 |
| 74LVT573DB | -40 °C to +85 °C | SSOP20 | plastic shrink small outline package; 20 leads; body width 5.3 mm | SOT339-1 |
| 74LVT573PW | -40 °C to +85 °C | TSSOP20 | plastic thin shrink small outline package; 20 leads; body width 4.4 mm | SOT360-1 |
| 74LVT573BQ | -40 °C to +85 °C | DHVQFN20 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm | SOT764-1 |

4. Functional diagram

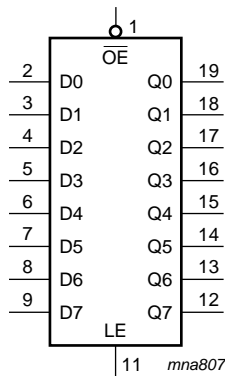


Fig 1. Logic symbol

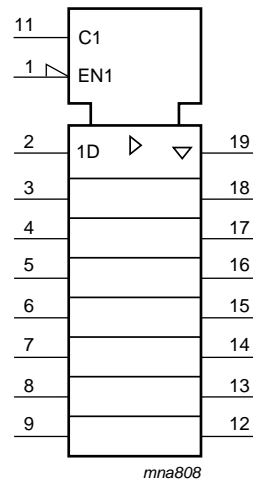


Fig 2. IEC logic symbol

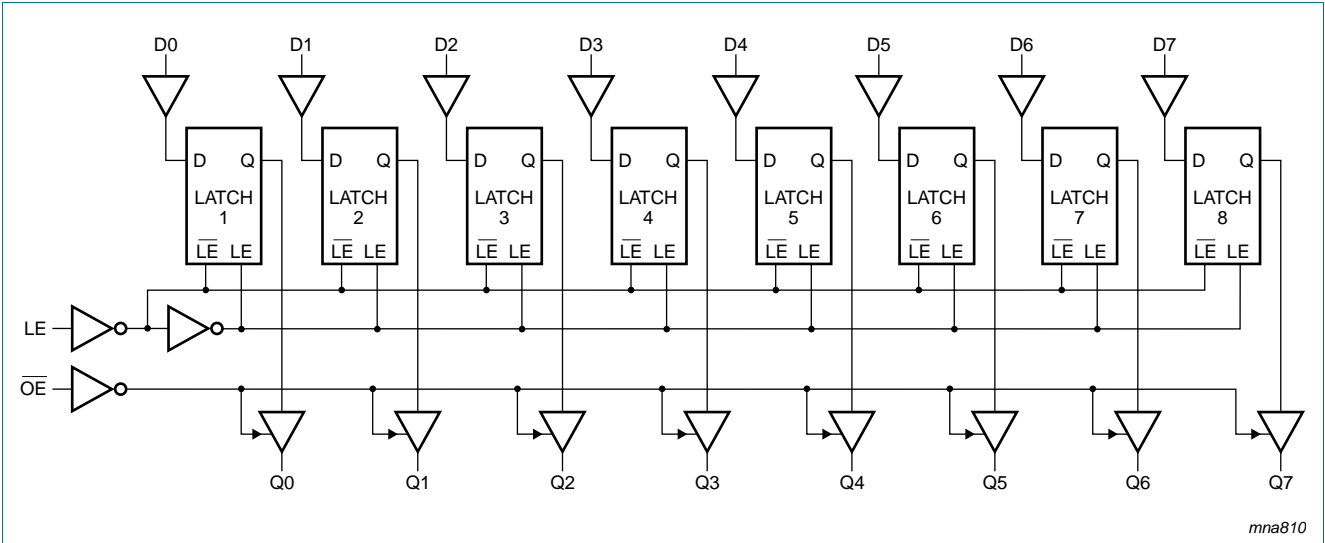


Fig 3. Logic diagram

5. Pinning information

5.1 Pinning

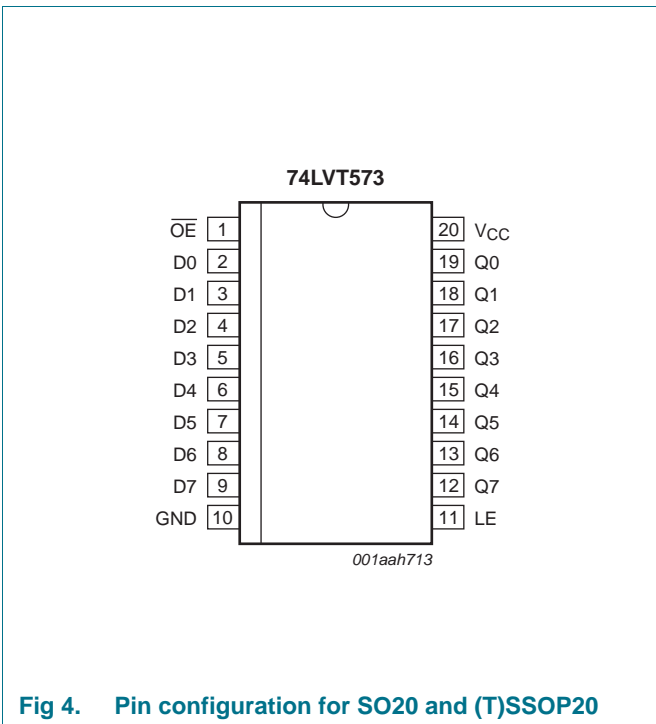
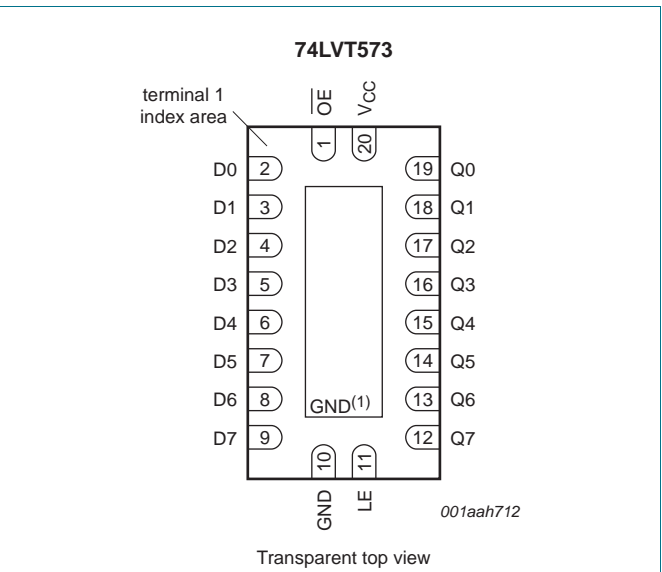


Fig 4. Pin configuration for SO20 and (T)SSOP20



- (1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig 5. Pin configuration for DHVQFN20

5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|-----------------|--------------------------------|----------------------------------|
| \overline{OE} | 1 | output enable input (active LOW) |
| D0 to D7 | 2, 3, 4, 5, 6, 7, 8, 9 | data input |
| GND | 10 | ground (0 V) |
| LE | 11 | latch enable (active HIGH) |
| Q0 to Q7 | 19, 18, 17, 16, 15, 14, 13, 12 | data output |
| V_{CC} | 20 | supply voltage |

6. Functional description

6.1 Function table

Table 3. Function table [\[1\]](#)

| Operating mode | Control \overline{OE} | Control LE | Input Dn | Internal register | Output Qn |
|-------------------------------|-------------------------|------------|----------|-------------------|-----------|
| Load and read register enable | L | H | L | L | L |
| | | | H | H | H |
| Latch and read register | L | ↓ | l | L | L |
| | | | h | H | H |
| Hold | L | L | X | NC | NC |
| Disable outputs | H | L | X | NC | Z |
| | | H | Dn | Dn | Z |

- [1] H = HIGH voltage level;
 L = LOW voltage level;
 ↓ = HIGH-to-LOW latch enable transition;
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition;
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition;
 Z = high-impedance OFF-state;
 NC = no change;
 X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|----------|-------------------------|-----------------------------------|--------------------------|------|------|
| V_{CC} | supply voltage | | -0.5 | +4.6 | V |
| V_I | input voltage | | [1] -0.5 | +7.0 | V |
| V_O | output voltage | output in OFF-state or HIGH-state | [1] -0.5 | +7.0 | V |
| I_{IK} | input clamping current | $V_I < 0$ V | - | -50 | mA |
| I_{OK} | output clamping current | $V_O < 0$ V | - | -50 | mA |
| I_O | output current | output in LOW-state | - | 128 | mA |
| | | output in HIGH-state | - | -64 | mA |

Table 4. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|-------------------------------------|-------|------|------|
| T _{stg} | storage temperature | | -65 | +150 | °C |
| T _j | junction temperature | | [2] - | 150 | °C |
| P _{tot} | total power dissipation | T _{amb} = -40 °C to +85 °C | [3] - | 500 | mW |

- [1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
- [2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.
- [3] For SO20 packages: above 70 °C derate linearly with 8 mW/K.
For SSOP20 and TSSOP20 packages: above 60 °C derate linearly with 5.5 mW/K.
For DHVQFN20 packages: above 60 °C derate linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|-------------------------------------|---|-----|-----|-----|------|
| V _{CC} | supply voltage | | 2.7 | - | 3.6 | V |
| V _i | input voltage | | 0 | - | 5.5 | V |
| V _{IH} | HIGH-level input voltage | | 2.0 | - | - | V |
| V _{IL} | LOW-level input voltage | | - | - | 0.8 | V |
| I _{OH} | HIGH-level output current | | - | - | -32 | mA |
| I _{OL} | LOW-level output current | | - | - | 32 | mA |
| | | current duty cycle ≤ 50 %; f _i ≥ 1 kHz | - | - | 64 | mA |
| T _{amb} | ambient temperature | in free air | -40 | - | +85 | °C |
| Δt/ΔV | input transition rise and fall rate | outputs enabled | - | - | 10 | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | T _{amb} = -40 °C to +85 °C | | | Unit |
|---------------------|-----------------------------------|--|-------------------------------------|-----------------------|------|------|
| | | | Min | Typ ^[1] | Max | |
| V _{IK} | input clamping voltage | V _{CC} = 2.7 V; I _{IK} = -18 mA | -1.2 | -0.9 | - | V |
| V _{OH} | HIGH-level output voltage | V _{CC} = 2.7 V to 3.6 V; I _{OH} = -100 μA | V _{CC} - 0.2 | V _{CC} - 0.1 | - | V |
| | | V _{CC} = 2.7 V; I _{OH} = -8 mA | 2.4 | 2.5 | - | V |
| | | V _{CC} = 3.0 V; I _{OH} = -32 mA | 2.0 | 2.2 | - | V |
| V _{OL} | LOW-level output voltage | V _{CC} = 2.7 V; I _{OL} = 100 μA | - | 0.1 | 0.2 | V |
| | | V _{CC} = 2.7 V; I _{OL} = 24 mA | - | 0.3 | 0.5 | V |
| | | V _{CC} = 3.0 V I _{OL} = 16 mA | - | 0.25 | 0.4 | V |
| | | V _{CC} = 3.0 V I _{OL} = 32 mA | - | 0.3 | 0.5 | V |
| | | V _{CC} = 3.0 V I _{OL} = 64 mA | - | 0.4 | 0.55 | V |
| V _{OL(pu)} | power-up LOW-level output voltage | V _{CC} = 3.6 V; I _O = 1 mA; V _i = GND or V _{CC} | [2] - | 0.13 | 0.55 | V |

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | T _{amb} = -40 °C to +85 °C | | | Unit |
|-----------------------|------------------------------------|--|-------------------------------------|--------------------|------|------|
| | | | Min | Typ ^[1] | Max | |
| I _I | input leakage current | all input pins; | | | | |
| | | V _{CC} = 0 V or 3.6 V; V _I = 5.5 V | - | 1 | 10 | μA |
| | | control pins; | | | | |
| | | V _{CC} = 3.6 V; V _{CC} or GND | - | ±0.1 | ±1 | μA |
| I _{OFF} | power-off leakage current | data pins | | | | |
| | | V _{CC} = 3.6 V; V _I = V _{CC} ^[3] | - | 0.1 | 1 | μA |
| | | V _{CC} = 3.6 V; V _I = 0 V | -5 | -1 | - | μA |
| I _{BHL} | bus hold LOW current | V _{CC} = 0 V; V _I or V _O = 0 V to 4.5 V | - | 1 | ±100 | μA |
| I _{BHH} | bus hold HIGH current | Dn input; V _{CC} = 3 V; V _I = 0.8 V ^[4] | 75 | 150 | - | μA |
| I _{BHHO} | bus hold HIGH overdrive current | Dn input; V _{CC} = 3 V; V _I = 2.0 V | - | -150 | -75 | μA |
| I _{BHLO} | bus hold LOW overdrive current | Dn input; V _{CC} = 3.6; V _I = 0 V to 3.6 V ^[4] | - | - | 500 | μA |
| I _{BHLO} | bus hold LOW overdrive current | Dn input; V _{CC} = 3.6; V _I = 0 V to 3.6 V | -500 | - | - | μA |
| I _{LO} | output leakage current | Qn output HIGH when V _O = 5.5 V and V _{CC} = 3.0 V | - | 60 | 125 | μA |
| I _{O(pu/pd)} | power-up/power-down output current | V _{CC} ≤ 1.2 V; V _O = 0.5 V to V _{CC} ; V _I = GND or V _{CC} ; \overline{OE} = don't care ^[5] | - | 1 | ±100 | μA |
| I _{OZ} | OFF-state output current | V _{CC} = 3.6 V; V _I = V _{IH} or V _{IL} | | | | |
| | | output HIGH: V _O = 3.0 V | - | 1 | 5 | μA |
| | | output LOW: V _O = 0.5 V | -5 | -1 | - | μA |
| I _{CC} | supply current | V _{CC} = 3.6 V; V _I = GND or V _{CC} ; I _O = 0 A | | | | |
| | | outputs HIGH | - | 0.13 | 0.19 | mA |
| | | outputs LOW | - | 3 | 12 | mA |
| | | outputs disabled ^[6] | - | 0.13 | 0.19 | mA |
| ΔI _{CC} | additional supply current | per input pin; V _{CC} = 3 V to 3.6 V; one input at V _{CC} - 0.6 V and other inputs at V _{CC} or GND ^[7] | - | 0.1 | 0.2 | mA |
| C _I | input capacitance | V _I = 0 V or 3.0 V | - | 4 | - | pF |
| C _O | output capacitance | outputs disabled; V _O = 0 V or 3.0 V | - | 8 | - | pF |

- [1] Typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.
- [2] For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
- [3] Unused pins at V_{CC} or GND.
- [4] This is the bus hold overdrive current required to force the input to the opposite logic state.
- [5] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 μs is permitted. This parameter is valid for T_{amb} = 25 °C only.
- [6] I_{CC} is measured with outputs pulled to V_{CC} or GND.
- [7] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to ground (GND = 0 V); for test circuit see [Figure 11](#).

| Symbol | Parameter | Conditions | T _{amb} = -40 °C to +85 °C | | | Unit |
|------------------|-------------------------------------|--|-------------------------------------|--------------------|-----|------|
| | | | Min | Typ ^[1] | Max | |
| t _{PLH} | LOW to HIGH propagation delay | LE to Qn; see Figure 6 | | | | |
| | | V _{CC} = 3.0 V to 3.6 V | 1.6 | 3.5 | 5.6 | ns |
| | | V _{CC} = 2.7 V | - | - | 6.3 | ns |
| | | Dn to Qn; see Figure 7 | | | | |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | 2.5 | 4.2 | ns |
| | | V _{CC} = 2.7 V | - | - | 4.7 | ns |
| t _{PHL} | HIGH to LOW propagation delay | LE to Qn; see Figure 6 | | | | |
| | | V _{CC} = 3.0 V to 3.6 V | 2.5 | 4.3 | 6.5 | ns |
| | | V _{CC} = 2.7 V | - | - | 7.2 | ns |
| | | Dn to Qn; see Figure 7 | | | | |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | 2.7 | 4.3 | ns |
| | | V _{CC} = 2.7 V | - | - | 5.2 | ns |
| t _{PZH} | OFF-state to HIGH propagation delay | \overline{OE} to Qn; see Figure 8 | | | | |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | 2.8 | 5.1 | ns |
| t _{PZH} | OFF-state to HIGH propagation delay | V _{CC} = 2.7 V | - | - | 6.2 | ns |
| | | \overline{OE} to Qn; see Figure 9 | | | | |
| t _{PZL} | OFF-state to LOW propagation delay | V _{CC} = 3.0 V to 3.6 V | 1.3 | 3.3 | 5.5 | ns |
| | | V _{CC} = 2.7 V | - | - | 6.6 | ns |
| t _{PHZ} | HIGH to OFF-state propagation delay | \overline{OE} to Qn; see Figure 8 | | | | |
| | | V _{CC} = 3.0 V to 3.6 V | 2.0 | 3.7 | 5.7 | ns |
| t _{PHZ} | HIGH to OFF-state propagation delay | V _{CC} = 2.7 V | - | - | 6.7 | ns |
| | | \overline{OE} to Qn; see Figure 9 | | | | |
| t _{PLZ} | LOW to OFF-state propagation delay | V _{CC} = 3.0 V to 3.6 V | 1.5 | 3.0 | 4.6 | ns |
| | | V _{CC} = 2.7 V | - | - | 5.1 | ns |
| t _{su} | set-up time | Dn to LE; see Figure 10 ^[2] | | | | |
| | | V _{CC} = 3.0 V to 3.6 V | 0.7 | - | - | ns |
| | | V _{CC} = 2.7 V | 0.6 | - | - | ns |
| t _h | hold time | Dn to LE; see Figure 10 ^[3] | | | | |
| | | V _{CC} = 3.0 V to 3.6 V | 1.6 | - | - | ns |
| | | V _{CC} = 2.7 V | 1.8 | - | - | ns |
| t _w | pulse width | LE input HIGH; see Figure 6 ^[4] | | | | |
| | | V _{CC} = 3.0 V to 3.6 V | 3.3 | - | - | ns |
| | | V _{CC} = 2.7 V | 3.3 | - | - | ns |

[1] Typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.

[2] t_{su} is the same as t_{su(L)} and t_{su(H)}.

[3] t_h is the same as t_{h(L)} and t_{h(H)}.

[4] t_w is the same as t_{wL} and t_{wH}.

11. Waveforms

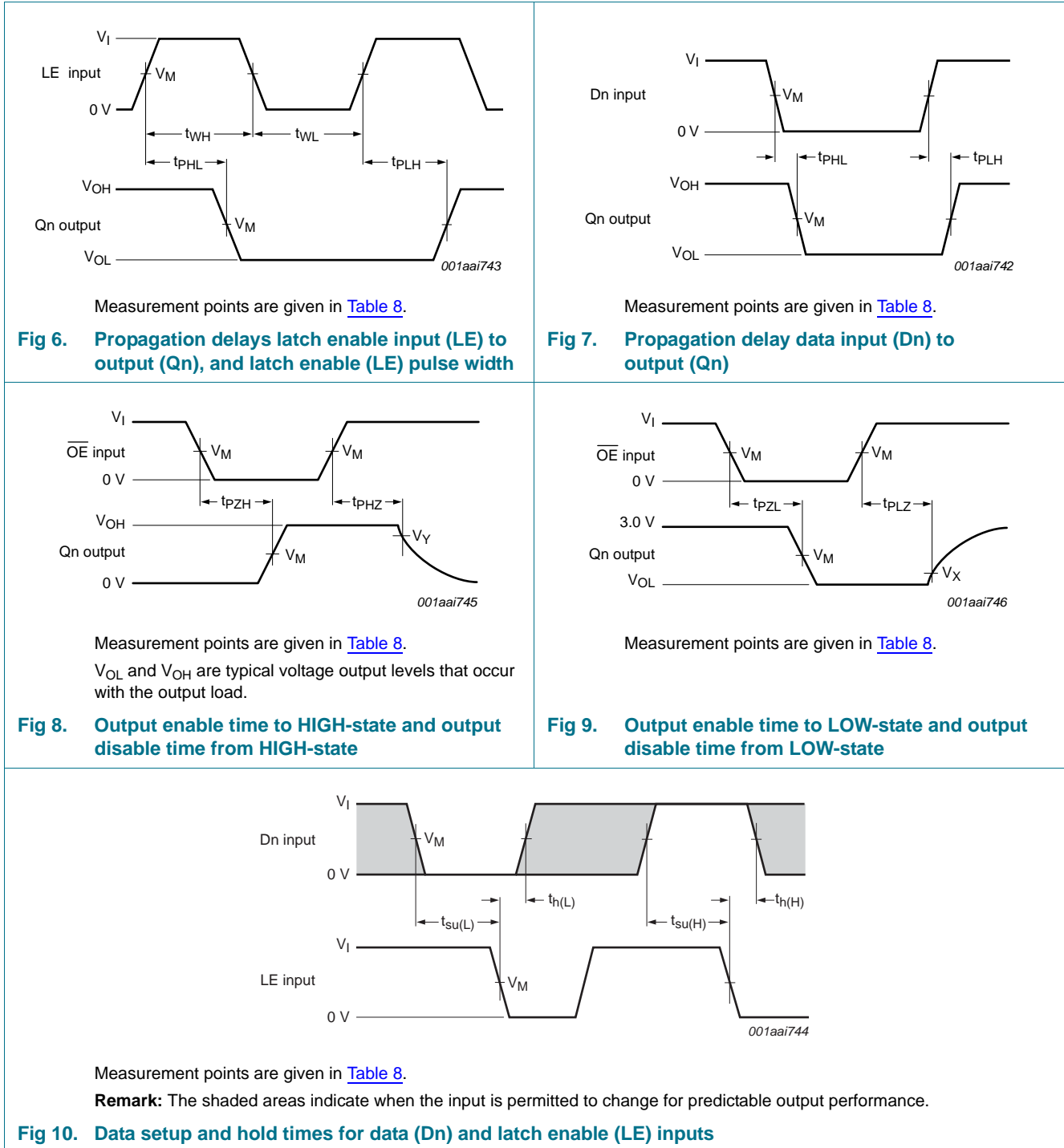
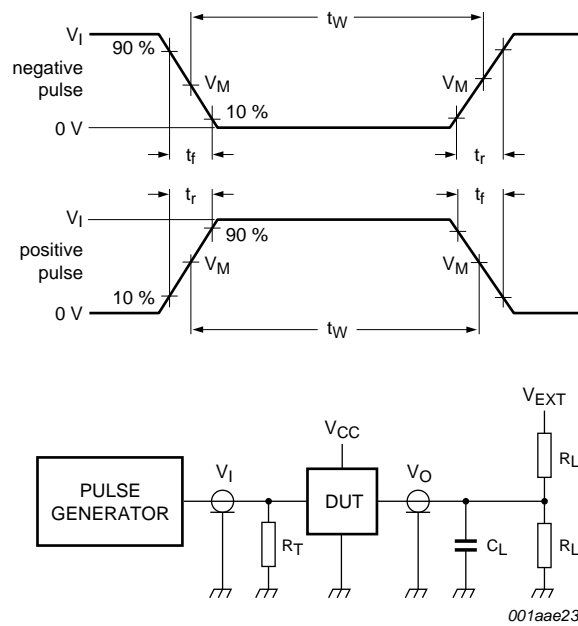


Table 8. Measurement points

| Input | Output | | |
|-------|--------|------------------|------------------|
| V_M | V_M | V_X | V_Y |
| 1.5 V | 1.5 V | $V_{OL} + 0.3 V$ | $V_{OH} - 0.3 V$ |



Test data is given in [Table 9](#).

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

Fig 11. Test circuitry for switching times

Table 9. Test data

| Input | | | | Load | | V_{EXT} | | |
|-------|---------------|--------|---------------|-------|--------------|--------------------|--------------------|--------------------|
| V_I | f_i | t_W | t_r, t_f | C_L | R_L | t_{PHZ}, t_{PZH} | t_{PLZ}, t_{PZL} | t_{PLH}, t_{PHL} |
| 2.7 V | ≤ 10 MHz | 500 ns | ≤ 2.5 ns | 50 pF | 500 Ω | GND | 6 V | open |

12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

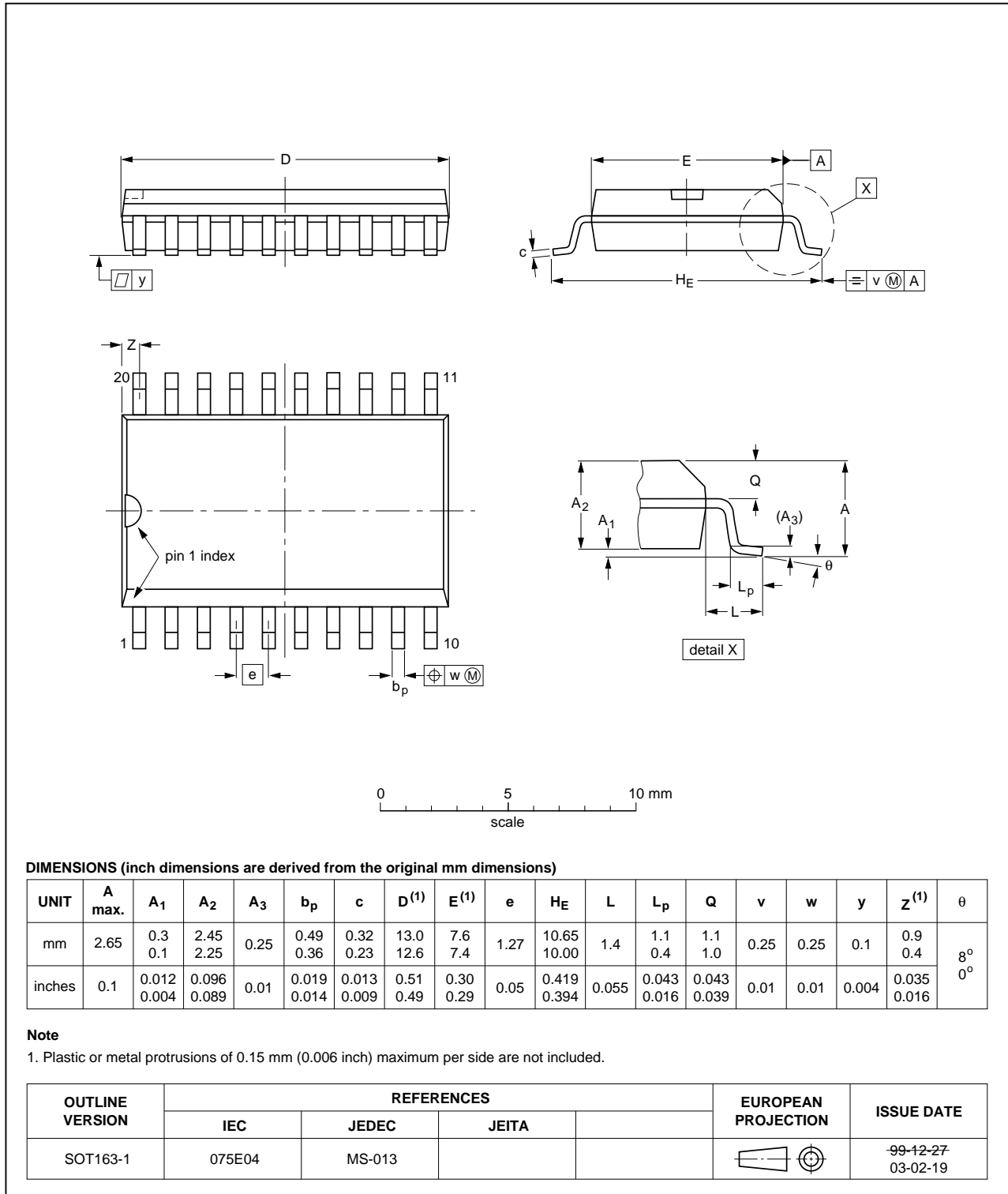


Fig 12. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

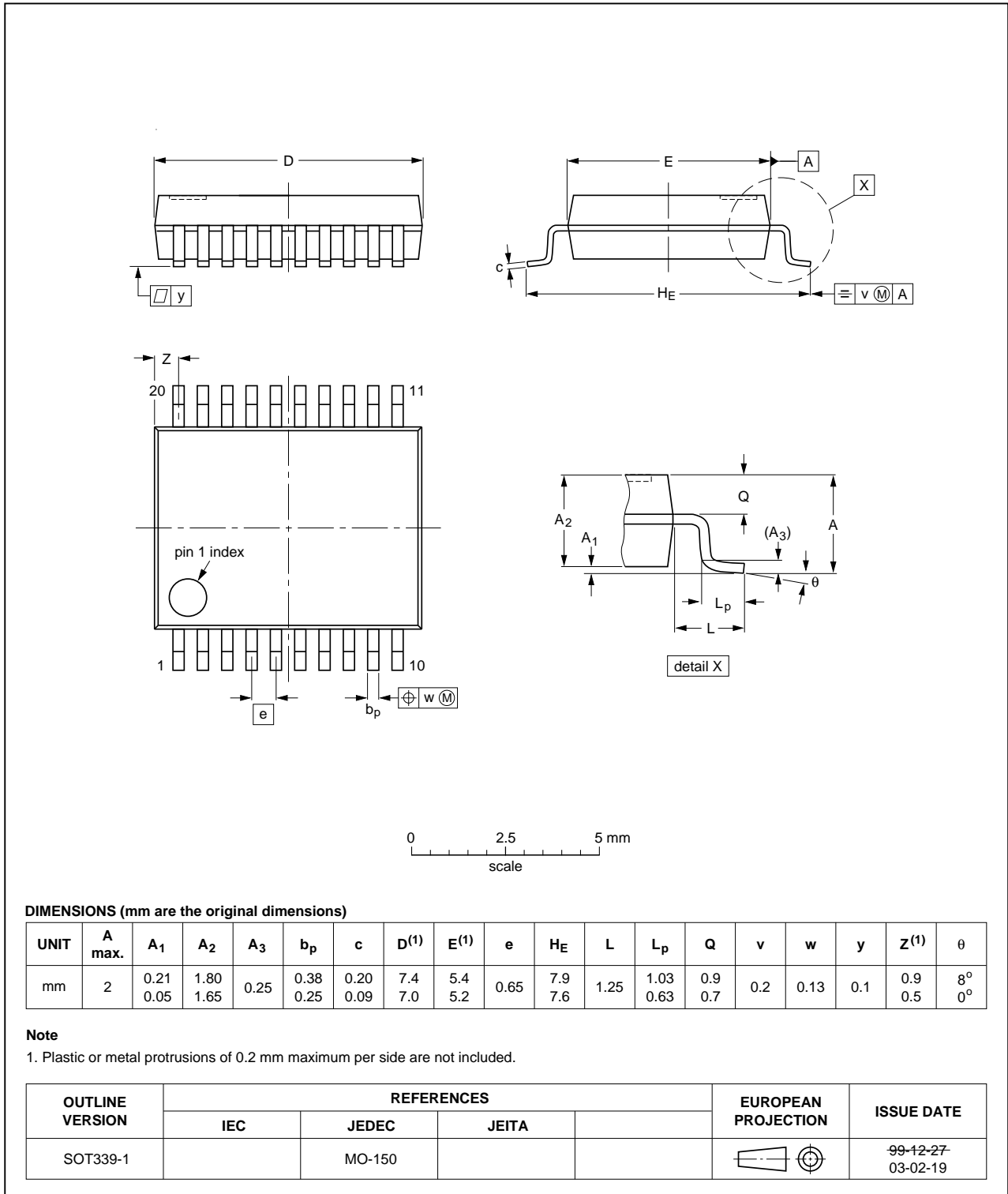


Fig 13. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



Fig 14. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

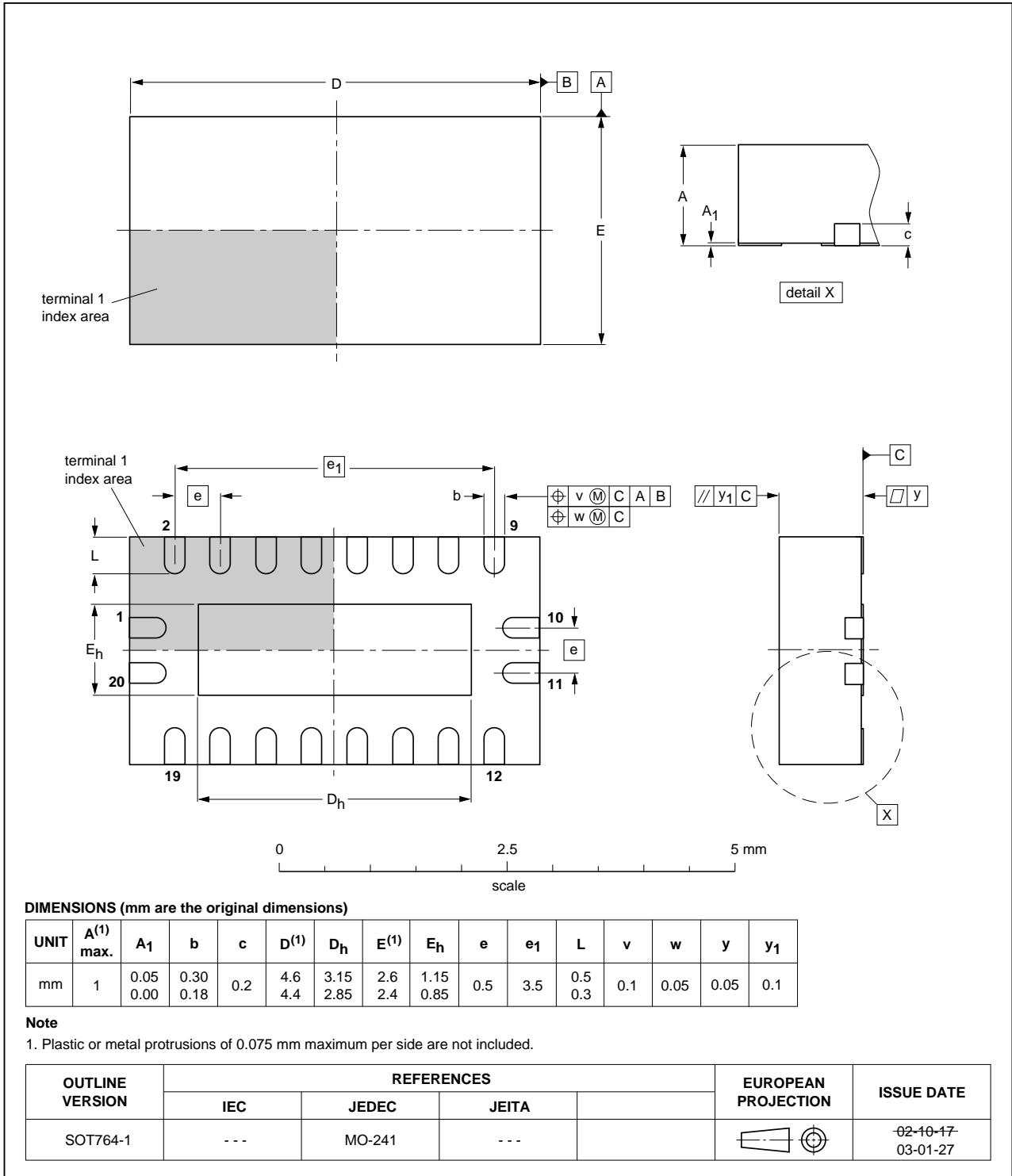


Fig 15. Package outline SOT764-1 (DHVQFN20)

13. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| BiCMOS | Bipolar Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

14. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|--|-----------------------|---------------|--------------|
| 74LVT573 v.8 | 20111122 | Product data sheet | - | 74LVT573 v.7 |
| Modifications: | <ul style="list-style-type: none"> Legal pages updated. | | | |
| 74LVT573 v.7 | 20110912 | Product data sheet | - | 74LVT573 v.6 |
| 74LVT573 v.6 | 20110727 | Product data sheet | - | 74LVT573 v.5 |
| 74LVT573 v.5 | 20110629 | Product data sheet | - | 74LVT573 v.4 |
| 74LVT573 v.4 | 20080915 | Product data sheet | - | 74LVT573 v.3 |
| 74LVT573 v.3 | 20011217 | Product data sheet | - | 74LVT573 v.2 |
| 74LVT573 v.2 | 19980219 | Product specification | - | - |

15. Legal information

15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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