C



A Schlumberger Company

MIL-STD-883 July 1986 — Rev 2⁵

μA139QB Quad Comparator

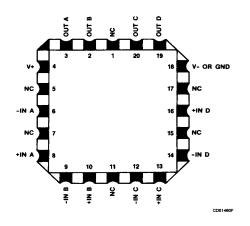
Aerospace and Defense Data Sheet Linear Products

Description

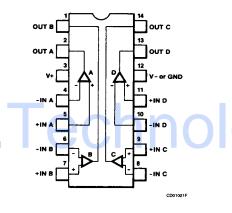
The μ A139QB consists of four independent precision voltage comparators designed specifically to operate from a single power supply. Operation from split power supplies is also possible and the low power supply current drain is independent of the supply voltage range. Darlington connected PNP input stages allow the input common mode voltage to include ground. 6

- Single Supply Operation
- Dual Supply Operation
- Allow Comparison Of Voltages Near Ground Potential
- Low Current Drain
- Compatible With All Forms Of Logic
- Low Input Bias Current
- Low Input Offset Current
- Low Offset Voltage

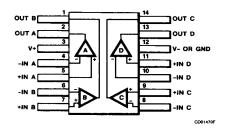
Connection Diagram 20-Terminal CCP (Top View)



Connection Diagram 14-Lead DIP (Top View)



Connection Diagram 14-Lead Flatpak (Top View)



Package Code

Order Information

Part No.	Finish	Mil-M-38510, Appendix
μA139FMQB	AA	F-1 (14-Lead Flatpak)
μA139DMQB	CA	D-1 (14-Lead DIP)
μA139LMQB	2C	C-2 (20-Terminal CCP)
JAN Product A	vailable	
11201	BCA	D-1 (14-Lead DIP)
11201	BCB	D-1 (14-Lead DIP)

μ A139QB

Absolute Maximum Ratings

Storage Temperature Range -65°C to 175°C Operating Temperature Range -55°C to 125°C 300°C Lead Temperature (soldering, 60 s) Internal Power Dissipation8 350 mW Flatpak DIP and CCP 400 mW ± 18 V or 36 V Supply Voltage Differential Input Voltage9 36 V -0.3 V to 36 V Input Voltage¹⁰

10 mA

Indefinite

Notes

- 1. 100% Test and Group A
- 2. Group A

Input Current Short Circuit Duration¹¹

- 3. Periodic tests, Group C
- 4. Guaranteed but not tested
- When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
- For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
- 7. VIR is guaranteed by the VIO test.
- Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 140°C/W for the Flatpak and 120°C/W for the DIP and CCP.
- 9. The differential input voltage shall not exceed the supply voltage.
- 10. For supply voltages less than ± 18 V, the absolute maximum input voltage is equal to the supply voltage. The input common mode voltage or either signal input voltage should not be allowed to go negative more than 0.3 V.
- 11. Short circuit may be to ground or negative supply. Rating applies to 125°C case temperature or 75°C ambient temperature. Short circuit from output to V+ can cause extensive heating and eventual destruction. No more than one amplifier should be shorted at the same time as the maximum junction temperature will be exceeded.

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

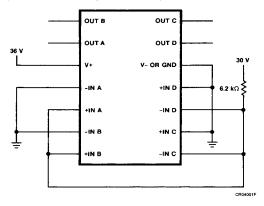
- 1. Static tests at 25°C
- 2. Static tests at 125°C
- 3. Static tests at -55°C
- 4. Dynamic tests at 25°C
- 5. Dynamic tests at 125°C
- 6. Dynamic tests at -55°C
- 9. AC tests at 25°C
- 10. AC tests at 125°C
- 11. AC tests at -55°C

Group C and D Endpoints: Group A, Subgroup 1

 μ A139QB Electrical Characteristics V+ = 5 V, V- = 0 V, unless otherwise specified.

Symbol	Characteristic	Con	dition	Min	Max	Unit	Note	Subgrp
V _{IO}	Input Offset Voltage	5.0 V \leq V + \leq 36 V, V _O = 1.4 V	0 V ≤ V _{CM} ≤ (V+) - 1.5 V		5.0	mV	1	1
			0 V ≤ V _{CM} ≤ (V+) - 2.0 V		9.0	m∨	1	2,3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage	25°C ≤ T _A ≤ 129			25	μV/°C	4	2
	Temperature Sensitivity	-55°C ≤ T _A ≤ 25°C			25	μV/°C	4	3
lio	Input Offset Current	V _{CM} = 0 V			25	nA	1	1
					100	nA	1	2,3
$\Delta I_{\text{IO}}/\Delta T$	Input Offset Current Temperature Sensitivity	25°C ≤ T _A ≤ 125°C			300	pA/°C	4	2
		-55°C ≤ T _A ≤ 25°C			400	pA/°C	4	3
l _{IB}	Input Bias Current	V _{CM} = 0 V		-100		nA	1	1
				-300		nA	1	2,3
lcc	Supply Current (Total)	V _{CC} = 5.0 V			2.0	mA	1	1,2
					3.0	mA	1	3
		V _{CC} = 30 V			3.0	mA	1	1,2
					4.0	mA	1	3
CMR	Common Mode Rejection	$V+ = 30 \text{ V}, R_S = 50 \Omega, V_{CM} = 28 \text{ V}$		76		dB	4	1,2,3
V _{IR}	Input Voltage Range	$5.0 \text{ V} \leq \text{V} + \leq 36 \text{ V},$ $\text{V}_{\text{O}} = 1.4 \text{ V}$		0	V+ -1.5	V	7	1
				0	V+ -2	V	7	2,3
I _{CEX}	CEX Output Leakage Current	$V_l + = 1.0 \text{ V}, V_{l-} = 0 \text{ V},$			200	nA	1	1
		V _O = 30 V		1.0	μΑ	1	2,3	
I _{IL} (±)	Input Leakage Current	$V_{CC} + 36 \text{ V}, V_{I} + 34 \text{ V}, 0V$ $V_{I}^{-} = 0V, 34 \text{ V}$ $V_{I}^{+} = 0 \text{ V}, V_{I}^{-} = 1.0 \text{ V},$ $V_{O} = 1.5 \text{ V}$ $V_{I}^{+} = 0 \text{ V}, V_{I}^{-} = 10 \text{ V},$ $I_{OL} = 4 \text{ mA}$		-500	500	ns	4	1,2,3
loL	Output Sink Current			6.0		mA	1	1
V _{LAT}	Voltage Latch (High Level Input)				400	mV	3	1
V _{OL}	Low Level Output Voltage	$V_{i}+=0$ V, $V_{i}-=1.0$ V, $I_{OL}=4.0$ mA			400	mV	1	1
					700	mV	1	2,3
A _{VS}	Large Signal Voltage Gain	$V+ = 15 V$, $R_L = 15 k\Omega$		25		V/mV	4	4,5,6
CS	Channel Separation	V+ = 30 V		80		dB	4	9
t _{PLH}	Propagation Delay to High	High $V_l = 100 \text{ mV},$ $R_L = 5.1 \text{ k}\Omega$	V _{OD} = 5.0 mV		7.0	μs	3	10
	Level				5.0	μs	3	9,11
			V _{OD} = 50 mV		1.2	μs	3	10
					0.8	μs	3	9,11
t _{PHL}	Propagation Delay to Low Level	$V_{l} = 100 \text{ mV},$ $R_{L} = 5.1 \text{ k}\Omega$	V _{OD} = 5.0 mV		3.0	μs	3	10
					2.5	μs	3	9,11
			V _{OD} = 50 mV		1.0	μs	3	10
					0.8	μs	3	9,11

Primary Burn-In Circuit (38510/11201 may be used by FSC as an alternate)



Equivalent Circuit (1/4 of circuit)

