

74LVC823A

9-bit D-type flip-flop with 5 V tolerant inputs/outputs; positive edge-trigger; 3-state

Rev. 02 — 10 May 2004

Product data sheet

1. General description

The 74LVC823A is a high performance, low-power, low-voltage Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. In 3-state operation, outputs can handle 5 V. This feature allows the use of these devices as translators in a mixed 3.3 V and 5 V environment.

The 74LVC823A is a 9-bit D-type flip-flop with common clock (pin CP), clock enable (pin \overline{CE}), master reset (pin \overline{MR}) and 3-state outputs (pins Qn) for bus-oriented applications. The 9 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition, provided pin \overline{CE} is LOW. When pin \overline{CE} is HIGH, the flip-flops hold their data. A LOW on pin \overline{MR} resets all flip-flops. When pin \overline{OE} is LOW, the contents of the 9 flip-flops is available at the outputs. When pin \overline{OE} is HIGH, the outputs go to the high-impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

2. Features

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Flow-through pin-out architecture
- 9-bit positive edge-triggered register
- Independent register and 3-state buffer operation
- Complies with JEDEC standard JESD8-B/JESD36
- ESD protection:
 - ◆ HBM EIA/JESD22-A114-B exceeds 2000 V
 - ◆ MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from 40 °C to +85 °C and -40 °C to +125 °C.

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3. Quick reference data

Table 1: Quick reference data

$GND = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; $t_r = t_f \leq 2.5\text{ ns}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHL} , t_{PLH}	propagation delay CP to Qn	$C_L = 50\text{ pF}$; $V_{CC} = 3.3\text{ V}$	-	3.7	-	ns
t_{PHL}	propagation delay MR to Qn	$C_L = 50\text{ pF}$; $V_{CC} = 3.3\text{ V}$	-	4.1	-	ns
f_{max}	maximum clock frequency	$C_L = 50\text{ pF}$; $V_{CC} = 3.3\text{ V}$	-	200	-	MHz
C_I	input capacitance		-	5.0	-	pF
C_{PD}	power dissipation capacitance per gate	$V_{CC} = 3.3\text{ V}$	[1] [2]	-	-	
		outputs enabled	-	17	-	pF
		outputs disabled	-	13	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = total load switching outputs;

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

[2] The condition is $V_I = GND$ to V_{CC} .

4. Ordering information

Table 2: Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC823AD	-40 °C to +125 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
74LVC823ADB	-40 °C to +125 °C	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
74LVC823APW	-40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
74LVC823ABQ	-40 °C to +125 °C	DHVQFN24	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 × 5.5 × 0.85 mm	SOT815-1

5. Functional diagram

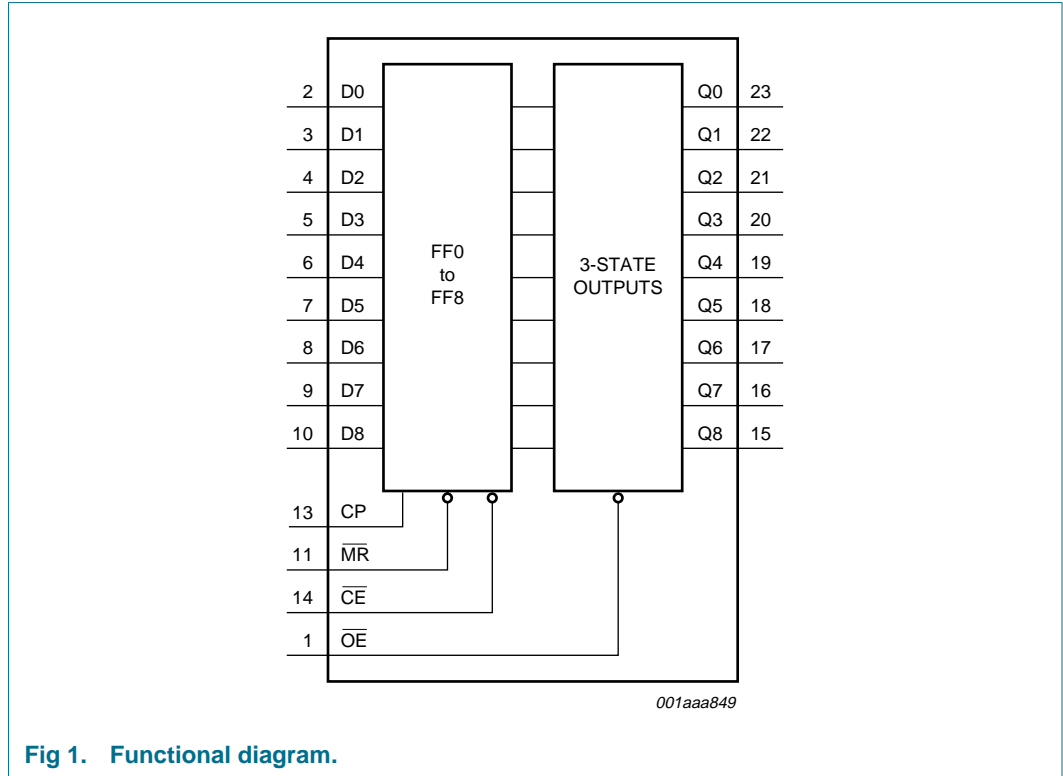


Fig 1. Functional diagram.

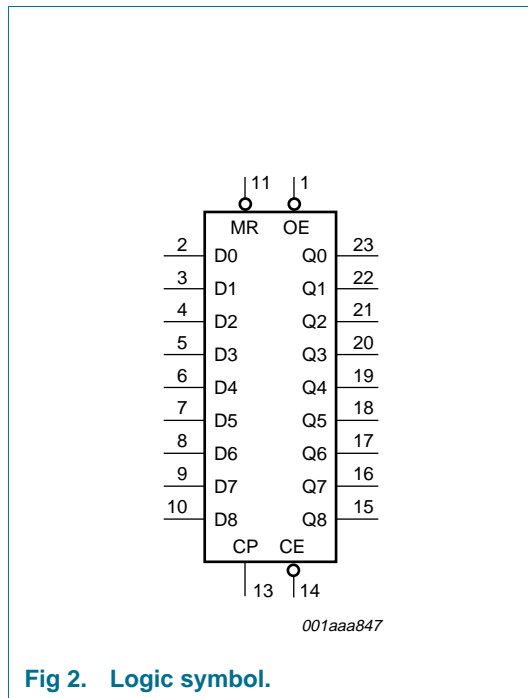


Fig 2. Logic symbol.

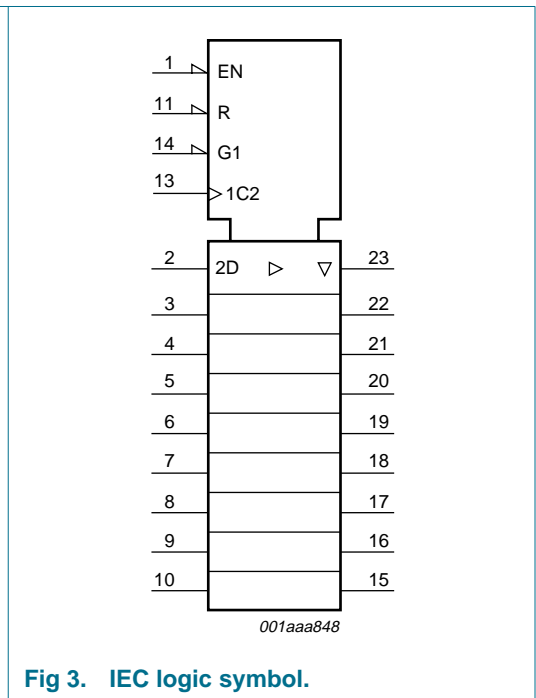


Fig 3. IEC logic symbol.

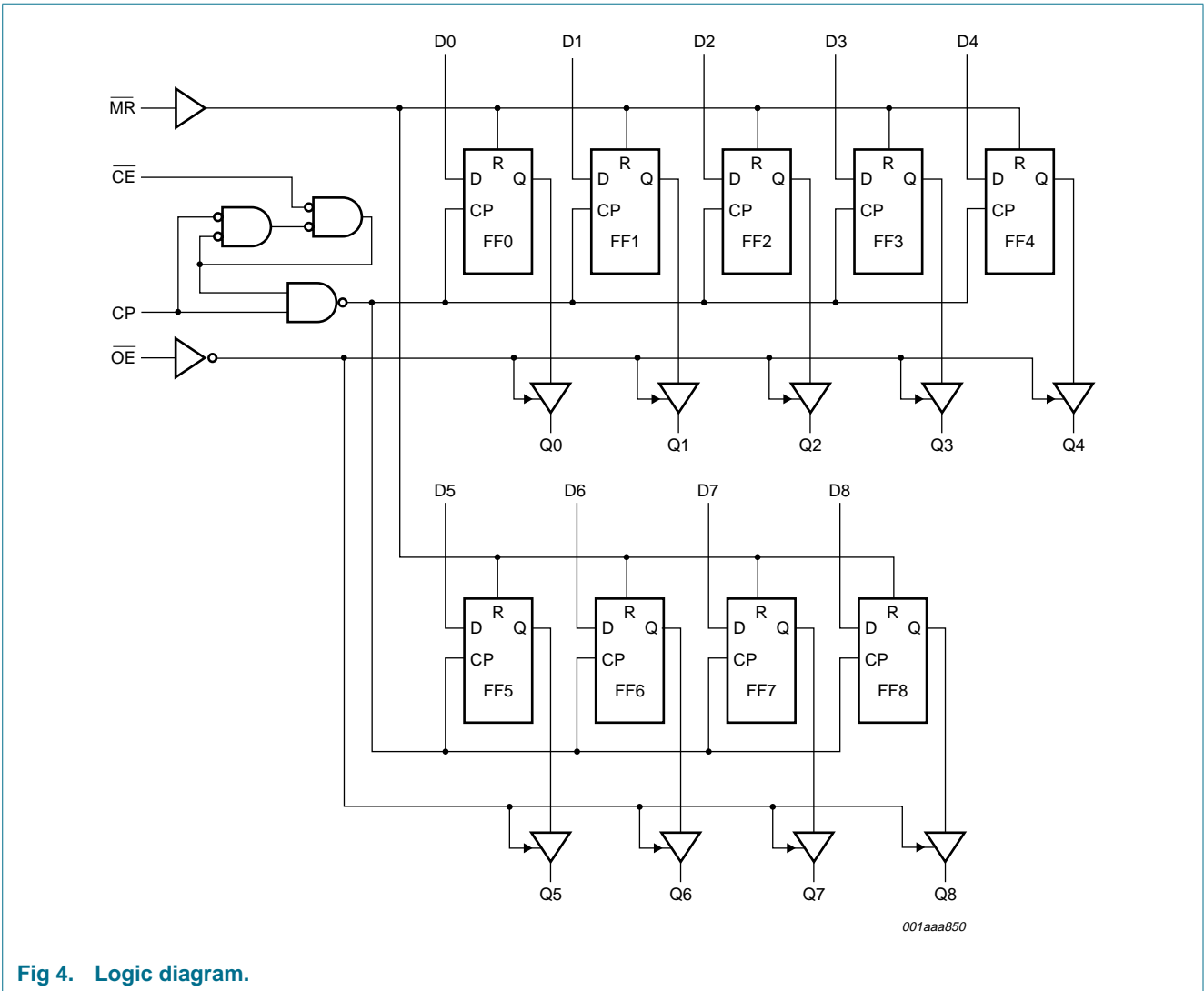
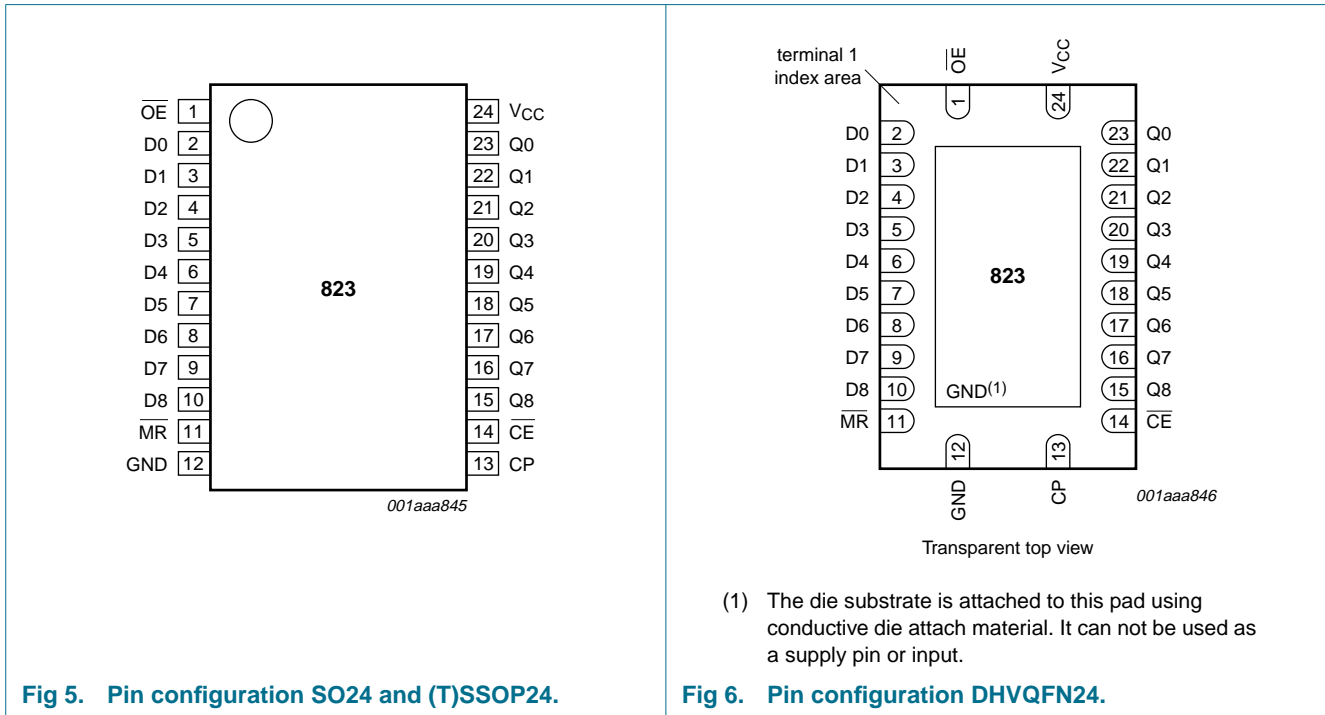


Fig 4. Logic diagram.

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
1	OE	output enable input (active LOW)
2	D0	data input
3	D1	data input
4	D2	data input
5	D3	data input
6	D4	data input
7	D5	data input
8	D6	data input
9	D7	data input
10	D8	data input
11	MR	master reset input (active LOW)
12	GND	ground (0 V)
13	CP	clock input (LOW-to-HIGH; edge-triggered)
14	CE	clock enable input (active LOW)
15	Q8	3-state flip-flop output
16	Q7	3-state flip-flop output
17	Q6	3-state flip-flop output

Table 3: Pin description ...continued

Symbol	Pin	Description
18	Q5	3-state flip-flop output
19	Q4	3-state flip-flop output
20	Q3	3-state flip-flop output
21	Q2	3-state flip-flop output
22	Q1	3-state flip-flop output
23	Q0	3-state flip-flop output
24	V _{CC}	supply voltage

7. Functional description

7.1 Function table

Table 4: Function table [1]

Operating mode	Input					Internal flip-flop	Output Q _n
	OE	MR	CE	CP	D _n		
Clear	L	L	X	X	X	L	L
Load and read register	L	H	L	↑	l	L	L
	L	H	L	↑	h	H	H
Load register and disable outputs	H	H	L	↑	l	L	Z
	H	H	L	↑	h	H	Z
Hold	L	H	H	NC	X	NC	NC

- [1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;
Z = high-impedance OFF-state;
NC = no change;
↑ = LOW-to-HIGH level transition;
X = don't care.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0$ V	-	-50	mA
V_I	input voltage		[1] -0.5	+6.5	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
V_O	output voltage	HIGH or LOW state	[1] -0.5	$V_{CC} + 0.5$	V
		3-state	[1] -0.5	+6.5	V
I_O	output source or sink current	$V_O = 0$ V to V_{CC}	-	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		-	±100	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	power dissipation	$T_{amb} = -40$ °C to +125 °C	[2] -	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO24 packages: P_{tot} derates linearly with 8 mW/K above 70 °C.

For SSOP24 and TSSOP24 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

For DHVQFN24 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	for maximum speed performance	2.7	-	3.6	V
		for low-voltage applications	1.2	-	3.6	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	HIGH or LOW state	0	-	V_{CC}	V
		3-state	0	-	5.5	V
T_{amb}	operating ambient temperature	in free air	-40	-	+125	°C
t_r, t_f	input rise and fall times	$V_{CC} = 1.2$ V to 2.7 V	0	-	20	ns/V
		$V_{CC} = 2.7$ V to 3.6 V	0	-	10	ns/V

10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = -40\text{ °C to }+85\text{ °C}$ [1]						
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.2\text{ V}$	V_{CC}	-	-	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.2\text{ V}$	-	-	GND	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$				
		$I_O = -100\text{ }\mu\text{A}; V_{CC} = 2.7\text{ V to }3.6\text{ V}$	[2] $V_{CC} - 0.2$	V_{CC}	-	V
		$I_O = -12\text{ mA}; V_{CC} = 2.7\text{ V}$	$V_{CC} - 0.5$	-	-	V
		$I_O = -18\text{ mA}; V_{CC} = 3.0\text{ V}$	$V_{CC} - 0.6$	-	-	V
		$I_O = -24\text{ mA}; V_{CC} = 3.0\text{ V}$	$V_{CC} - 0.8$	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$				
		$I_O = 100\text{ }\mu\text{A}; V_{CC} = 2.7\text{ V to }3.6\text{ V}$	[2] -	GND	0.2	V
		$I_O = 12\text{ mA}; V_{CC} = 2.7\text{ V}$	-	-	0.4	V
		$I_O = 24\text{ mA}; V_{CC} = 3.0\text{ V}$	-	-	0.55	V
I_{LI}	input leakage current	$V_I = 5.5\text{ V or GND}; V_{CC} = 3.6\text{ V}$	-	± 0.1	± 5	μA
I_{OZ}	3-state output OFF-state current	$V_I = V_{IH}\text{ or }V_{IL}; V_O = 5.5\text{ V or GND}; V_{CC} = 3.6\text{ V}$	-	0.1	± 5	μA
I_{off}	power-off leakage supply	$V_I\text{ or }V_O = 5.5\text{ V}; V_{CC} = 0\text{ V}$	-	0.1	± 10	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}\text{ or GND}; I_O = 0\text{ A}; V_{CC} = 3.6\text{ V}$	-	0.1	10	μA
ΔI_{CC}	additional quiescent supply current per pin	$V_I = V_{CC} - 0.6\text{ V}; I_O = 0\text{ A}; V_{CC} = 2.7\text{ V to }3.6\text{ V}$	[2] -	5	500	μA
C_I	input capacitance		-	5.0	-	pF
$T_{amb} = -40\text{ °C to }+125\text{ °C}$						
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.2\text{ V}$	V_{CC}	-	-	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.2\text{ V}$	-	-	GND	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$				
		$I_O = -100\text{ }\mu\text{A}; V_{CC} = 2.7\text{ V to }3.6\text{ V}$	$V_{CC} - 0.3$	-	-	V
		$I_O = -12\text{ mA}; V_{CC} = 2.7\text{ V}$	$V_{CC} - 0.65$	-	-	V
		$I_O = -18\text{ mA}; V_{CC} = 3.0\text{ V}$	$V_{CC} - 0.75$	-	-	V
		$I_O = -24\text{ mA}; V_{CC} = 3.0\text{ V}$	$V_{CC} - 1$	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$				
		$I_O = 100\text{ }\mu\text{A}; V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	0.3	V
		$I_O = 12\text{ mA}; V_{CC} = 2.7\text{ V}$	-	-	0.6	V
		$I_O = 24\text{ mA}; V_{CC} = 3.0\text{ V}$	-	-	0.8	V
I_{LI}	input leakage current	$V_I = 5.5\text{ V or GND}; V_{CC} = 3.6\text{ V}$	-	-	± 20	μA

Table 7: Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OZ}	3-state output OFF-state current	$V_I = V_{IH}$ or V_{IL} ; $V_O = 5.5$ V or GND; $V_{CC} = 3.6$ V	-	-	± 20	μA
I_{off}	power-off leakage supply	V_I or $V_O = 5.5$ V; $V_{CC} = 0$ V	-	-	± 20	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 3.6$ V	-	-	40	μA
ΔI_{CC}	additional quiescent supply current per pin	$V_I = V_{CC} - 0.6$ V; $I_O = 0$ A; $V_{CC} = 2.7$ V to 3.6 V	-	-	5000	μA

[1] All typical values are measured $T_{amb} = 25$ °C.[2] These typical values are measured at $V_{CC} = 3.3$ V.

11. Dynamic characteristics

Table 8: Dynamic characteristicsGND = 0 V; see [Figure 11](#) for test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = -40$ °C to $+85$ °C [1]						
t_{PHL} , t_{PLH}	propagation delay CP to Qn	see Figure 7 $V_{CC} = 1.2$ V	-	20	-	ns
		$V_{CC} = 2.7$ V	1.5	-	8.9	ns
		$V_{CC} = 3.0$ V to 3.6 V	[2] 1.5	3.7	8.0	ns
t_{PHL}	propagation delay \overline{MR} to Qn	see Figure 9 $V_{CC} = 1.2$ V	-	15	-	ns
		$V_{CC} = 2.7$ V	1.5	-	8.8	ns
		$V_{CC} = 3.0$ V to 3.6 V	[2] 1.5	4.1	7.9	ns
t_{PZH} , t_{PZL}	3-state output enable time \overline{OE} to Qn	see Figure 10 $V_{CC} = 1.2$ V	-	18	-	ns
		$V_{CC} = 2.7$ V	1.5	-	8.3	ns
		$V_{CC} = 3.0$ V to 3.6 V	[2] 1.5	3.3	7.2	ns
t_{PHZ} , t_{PLZ}	3-state output disable time \overline{OE} to Qn	see Figure 10 $V_{CC} = 1.2$ V	-	8.0	-	ns
		$V_{CC} = 2.7$ V	1.5	-	7.1	ns
		$V_{CC} = 3.0$ V to 3.6 V	[2] 1.5	2.9	6.0	ns
t_W	clock pulse width HIGH or LOW	see Figure 7 $V_{CC} = 2.7$ V	3.3	-	-	ns
		$V_{CC} = 3.0$ V to 3.6 V	[2] 3.3	1.7	-	ns
	master reset pulse width HIGH or LOW	see Figure 9 $V_{CC} = 2.7$ V	3.3	-	-	ns
		$V_{CC} = 3.0$ V to 3.6 V	[2] 3.3	1.7	-	ns

Table 8: Dynamic characteristics ...continued
GND = 0 V; see Figure 11 for test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{su}	set-up time Dn to CP	see Figure 8				
		$V_{CC} = 2.7\text{ V}$	1.8	-	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	[2] 1.3	0.0	-	ns
	set-up time \overline{CE} to CP	see Figure 8				
$V_{CC} = 2.7\text{ V}$		1.0	-	-	ns	
	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	[2] 1.8	-0.8	-	ns	
t_{rem}	removal time \overline{MR}	see Figure 9				
		$V_{CC} = 2.7\text{ V}$	2.0	-	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	[2] 1.0	-0.5	-	ns
t_h	hold time Dn to CP	see Figure 8				
		$V_{CC} = 2.7\text{ V}$	2.0	-	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	[2] 2.0	0.8	-	ns
	hold time \overline{CE} to CP	see Figure 8				
$V_{CC} = 2.7\text{ V}$		1.3	-	-	ns	
	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	[2] 1.3	0.0	-	ns	
f_{max}	maximum clock frequency	see Figure 7				
		$V_{CC} = 2.7\text{ V}$	150	-	-	MHz
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	[2] 150	200	-	MHz
$t_{sk(0)}$	skew	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	[3] -	-	1.0	ns
C_{PD}	power dissipation capacitance per gate	$V_{CC} = 3.3\text{ V}$	[4] [5] -	-	-	
		outputs enabled	-	17	-	pF
		outputs disabled	-	13	-	pF
$T_{amb} = -40\text{ °C to }+125\text{ °C}$						
t_{PHL}, t_{PLH}	propagation delay CP to Qn	see Figure 7				
		$V_{CC} = 2.7\text{ V}$	1.5	-	11.5	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.5	-	10.0	ns
t_{PHL}	propagation delay \overline{MR} to Qn	see Figure 9				
		$V_{CC} = 2.7\text{ V}$	1.5	-	11.0	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.5	-	10.0	ns
t_{PZH}, t_{PZL}	3-state output enable time \overline{OE} to Qn	see Figure 10				
		$V_{CC} = 2.7\text{ V}$	1.5	-	10.5	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.5	-	9.0	ns
t_{PHZ}, t_{PLZ}	3-state output disable time \overline{OE} to Qn	see Figure 10				
		$V_{CC} = 2.7\text{ V}$	1.5	-	9.0	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.5	-	7.5	ns

Table 8: Dynamic characteristics ...continued
GND = 0 V; see Figure 11 for test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{w}	clock pulse width HIGH or LOW	see Figure 7				
		$V_{CC} = 2.7 \text{ V}$	3.3	-	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	3.3	-	-	ns
	master reset pulse width HIGH or LOW	see Figure 9				
		$V_{CC} = 2.7 \text{ V}$	3.3	-	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	3.3	-	-	ns
t_{su}	set-up time Dn to CP	see Figure 8				
		$V_{CC} = 2.7 \text{ V}$	1.8	-	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.3	-	-	ns
	set-up time \overline{CE} to CP	see Figure 8				
		$V_{CC} = 2.7 \text{ V}$	1.0	-	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.8	-	-	ns
t_{rem}	removal time MR	see Figure 9				
		$V_{CC} = 2.7 \text{ V}$	2.0	-	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	-	-	ns
t_h	hold time Dn to CP	see Figure 8				
		$V_{CC} = 2.7 \text{ V}$	2.0	-	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	2.0	-	-	ns
	hold time \overline{CE} to CP	see Figure 8				
		$V_{CC} = 2.7 \text{ V}$	1.3	-	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.3	-	-	ns
f_{max}	maximum clock frequency	see Figure 7				
		$V_{CC} = 2.7 \text{ V}$	150	-	-	MHz
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	150	-	-	MHz
$t_{sk(0)}$	skew	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	[3]	-	-	1.5 ns

[1] All typical values are measured $T_{amb} = 25 \text{ }^\circ\text{C}$.

[2] These typical values are measured at $V_{CC} = 3.3 \text{ V}$.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

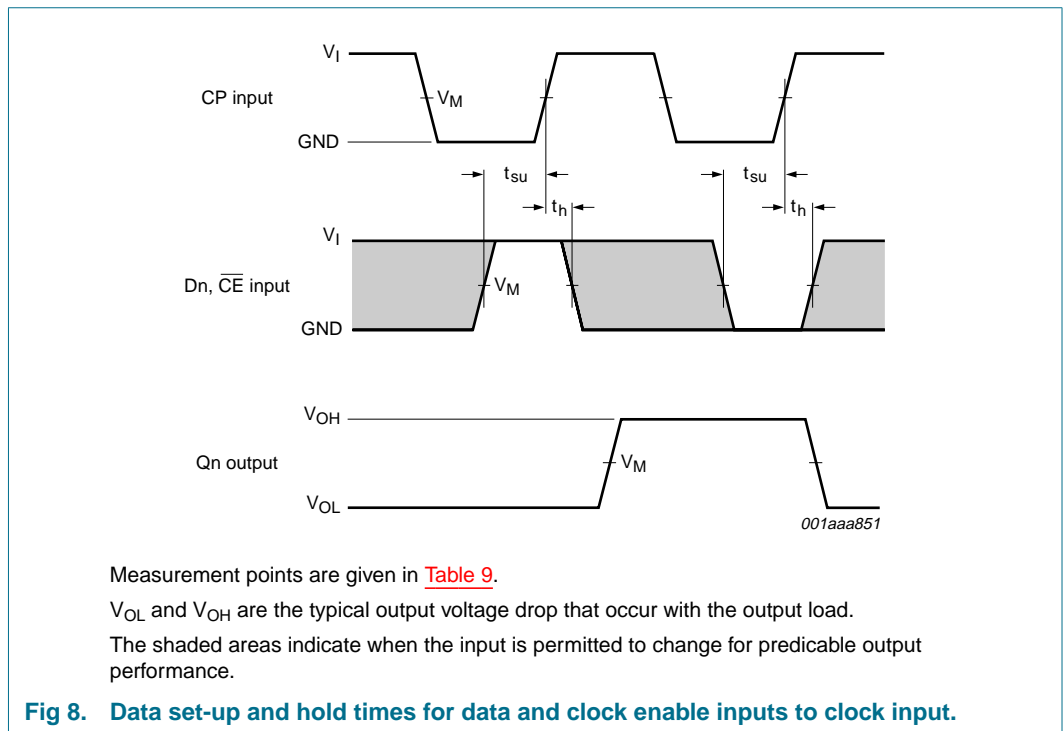
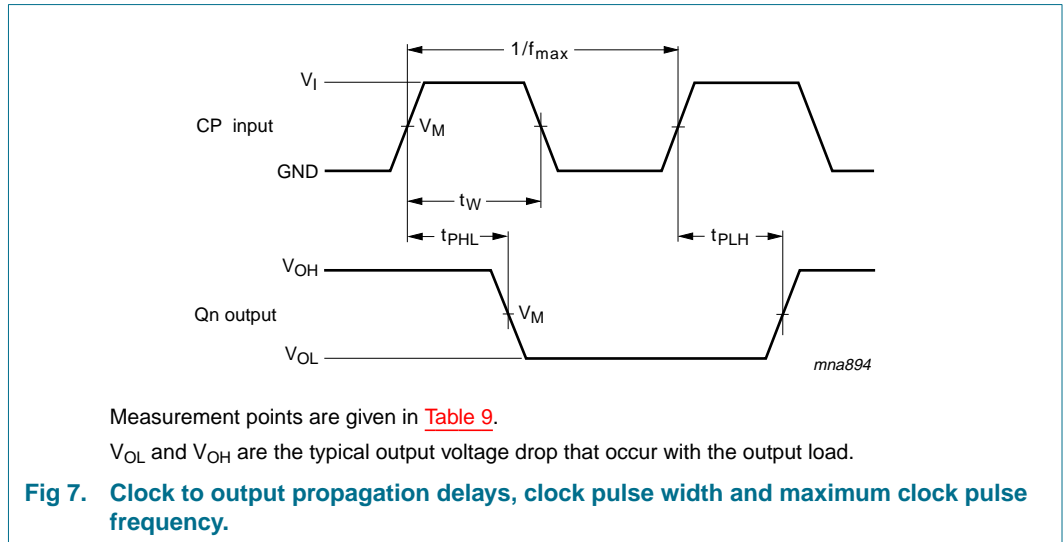
V_{CC} = supply voltage in V;

N = total load switching outputs;

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

[5] The condition is $V_I = \text{GND to } V_{CC}$.

12. Waveforms



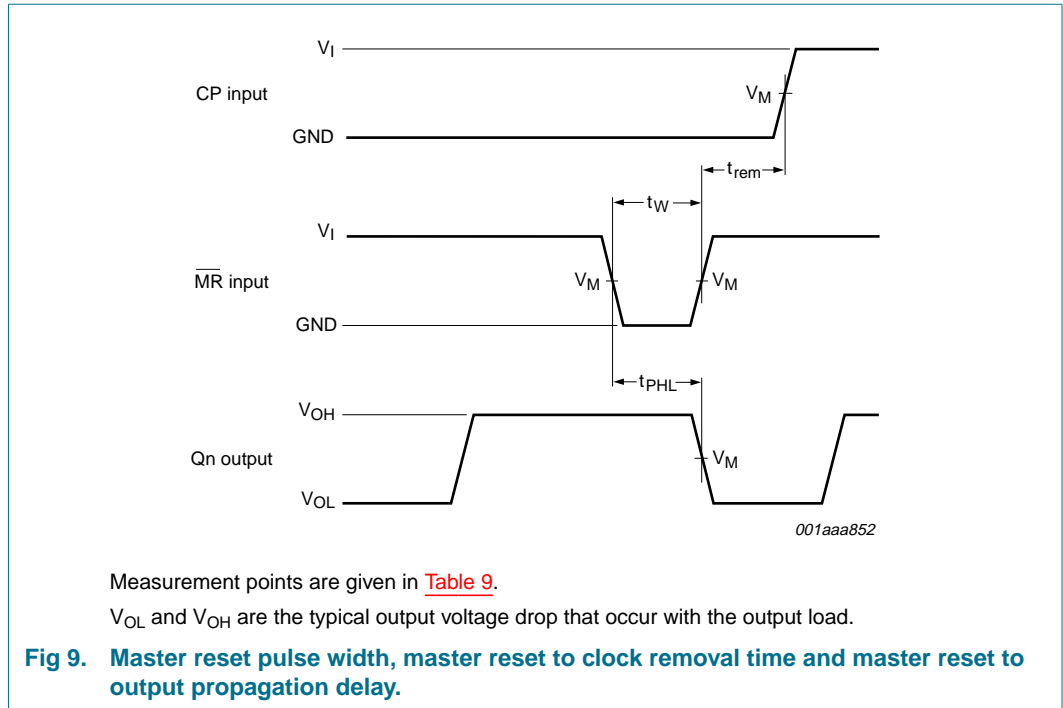


Table 9: Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.2 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V

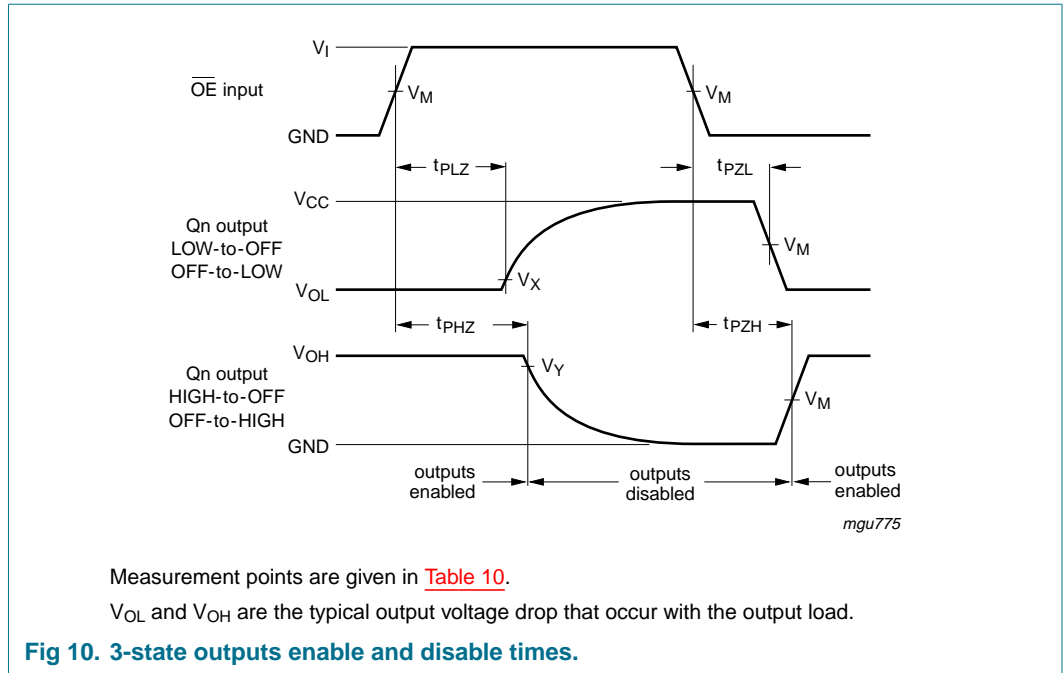


Table 10: Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
1.2 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.1 \text{ V}$	$V_{OH} - 0.1 \text{ V}$
2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$

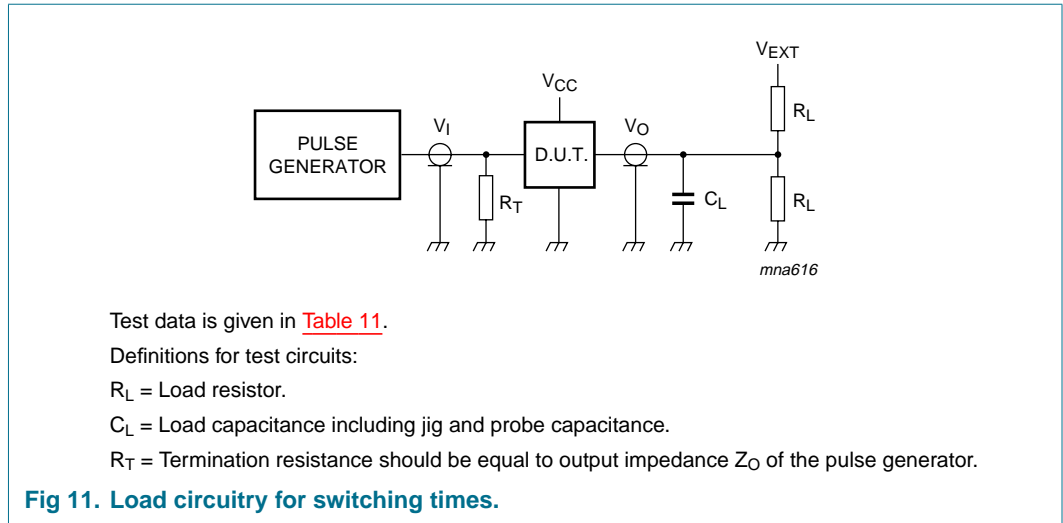


Table 11: Test data

Supply voltage	Input	Load		V_{EXT}		
V_{CC}	V_I	C_L	R_L	t_{PLH} , t_{PHL}	t_{PZH} , t_{PHZ}	t_{PZL} , t_{PLZ}
1.2 V	V_{CC}	50 pF	500 Ω [1]	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	50 pF	500 Ω	open	GND	$2 \times V_{CC}$
3.0 V to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	$2 \times V_{CC}$

[1] The circuit performs better when $R_L = 1000 \Omega$.

13. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

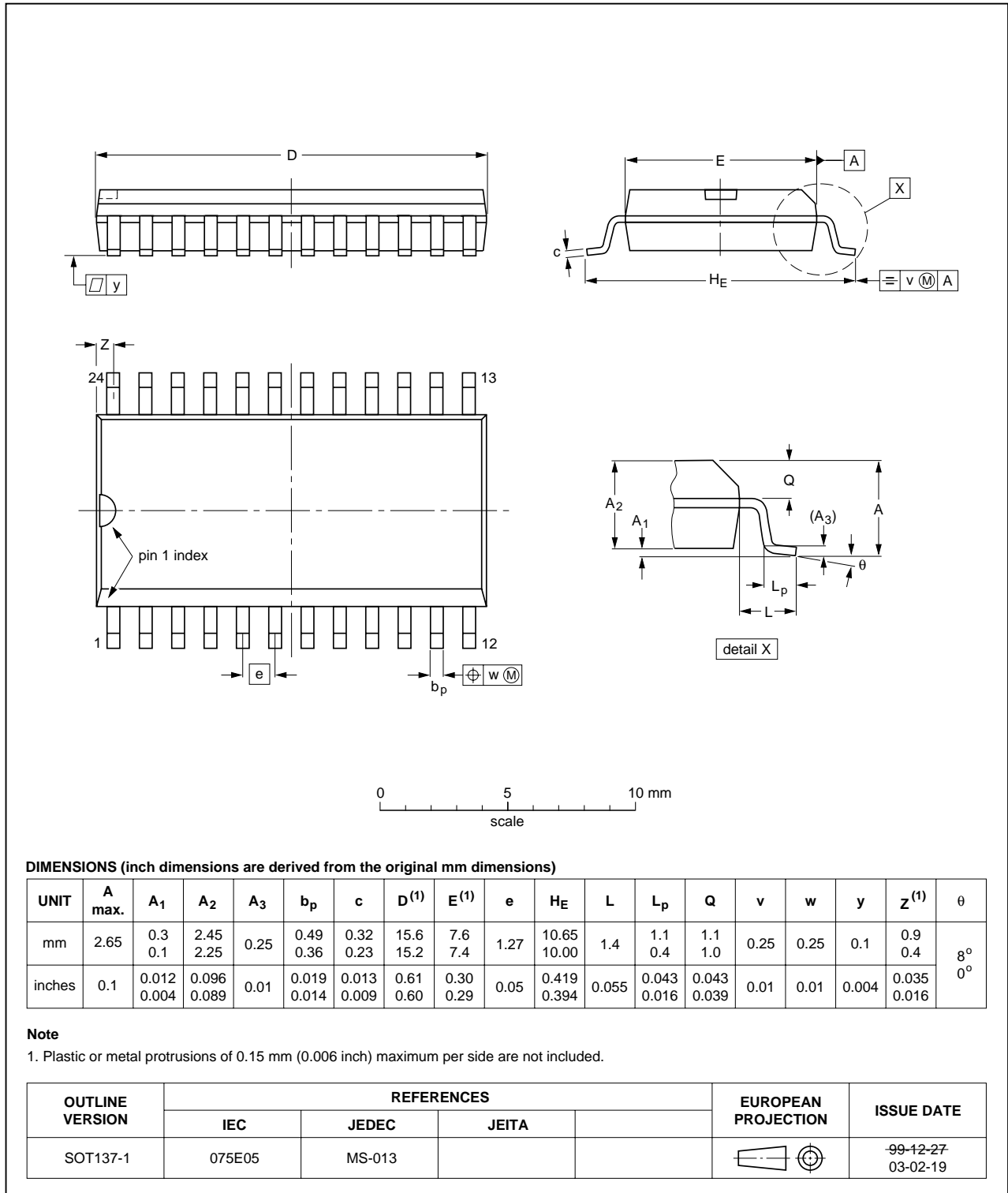


Fig 12. Package outline SO24.

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1

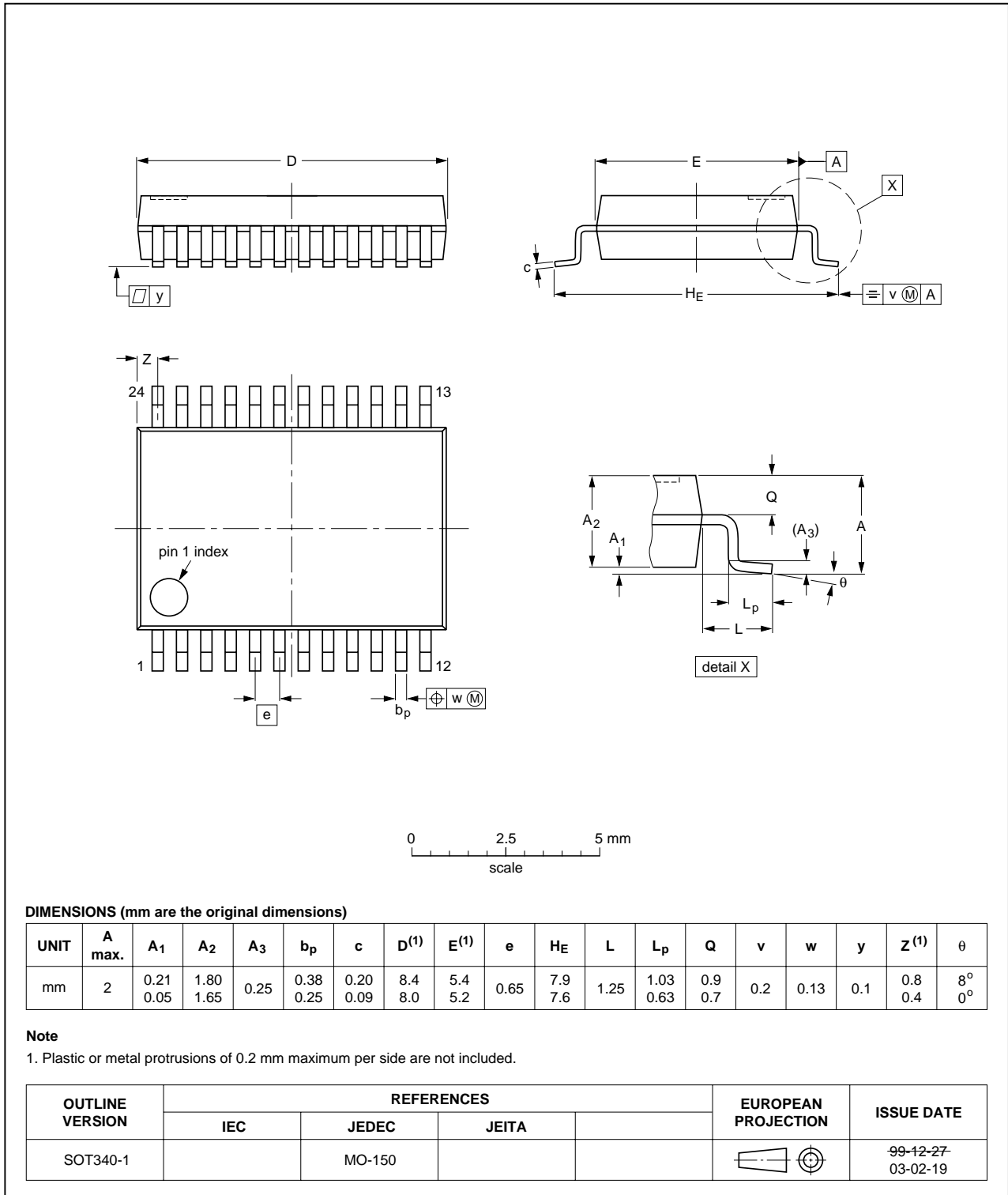


Fig 13. Package outline SSOP24.

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

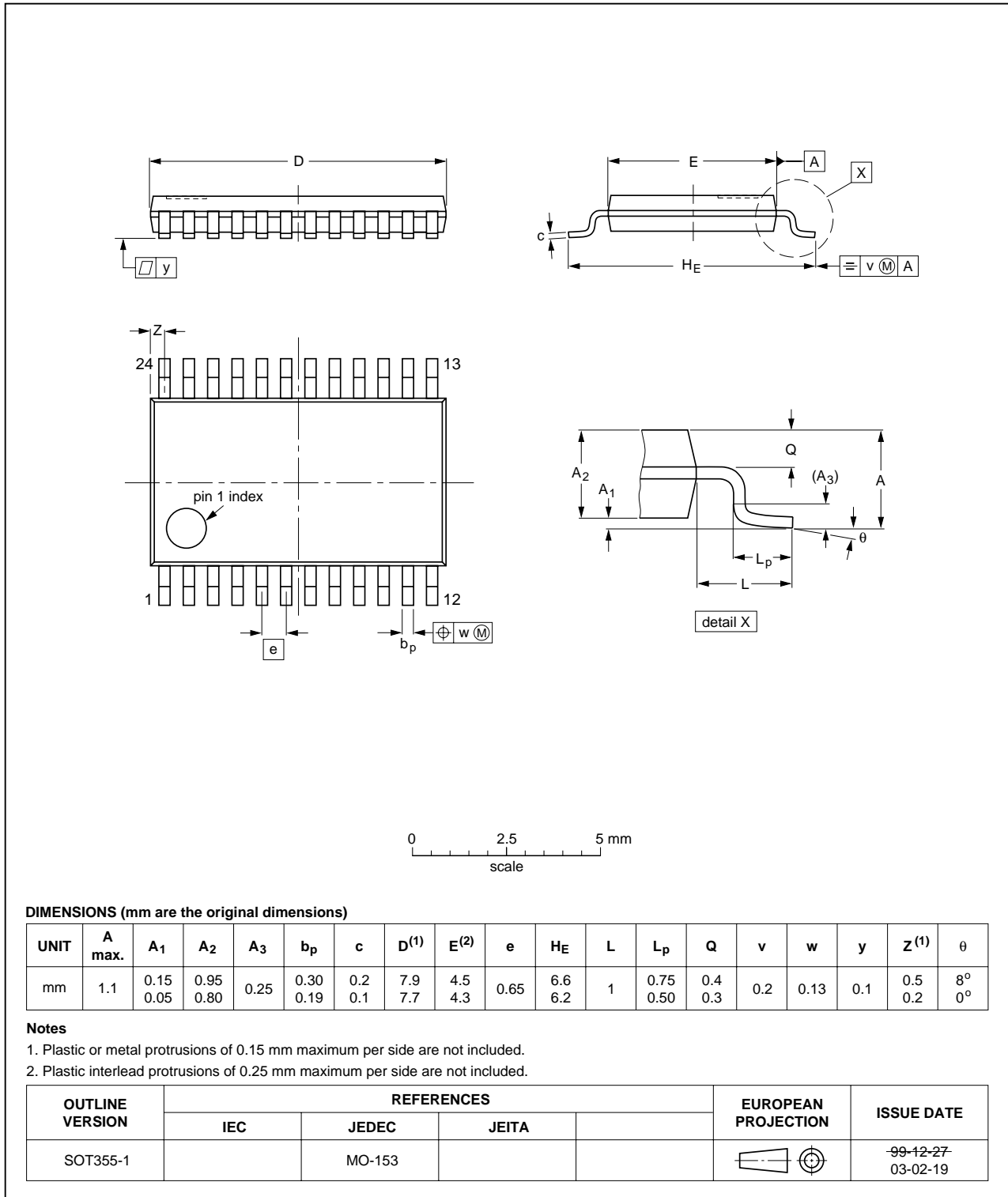


Fig 14. Package outline TSSOP24.

DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm

SOT815-1

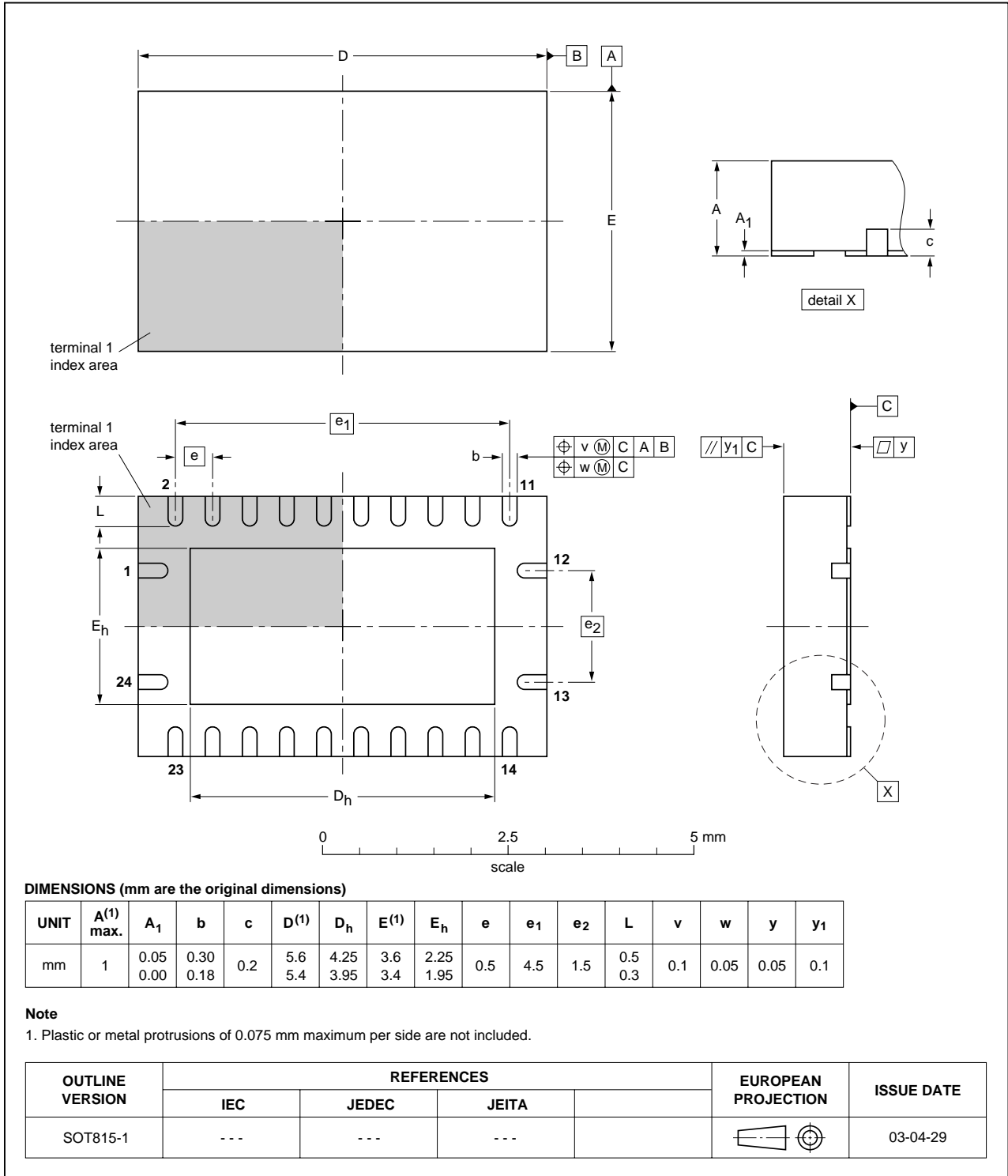


Fig 15. Package outline DHVQFN24.

14. Revision history

Table 12: Revision history

Document ID	Release date	Data sheet status	Change notice	Order number	Supersedes
74LVC823A_2	20040510	Product data	-	9397 750 13128	74LVC823A_1
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the current presentation and information standard of Philips Semiconductors. Table 2: added type number of DHVQFN24 package Figure 6: added pin configuration DHVQFN24 Table 7: added values for $T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ Table 8: added values for $T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$. 				
74LVC823A_1	19980924	Product specification	-	9397 750 04583	-

15. Data sheet status

Level	Data sheet status ^[1]	Product status ^[2] ^[3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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18. Contact information

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For sales office addresses, send an email to: sales.addresses@www.semiconductors.philips.com

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